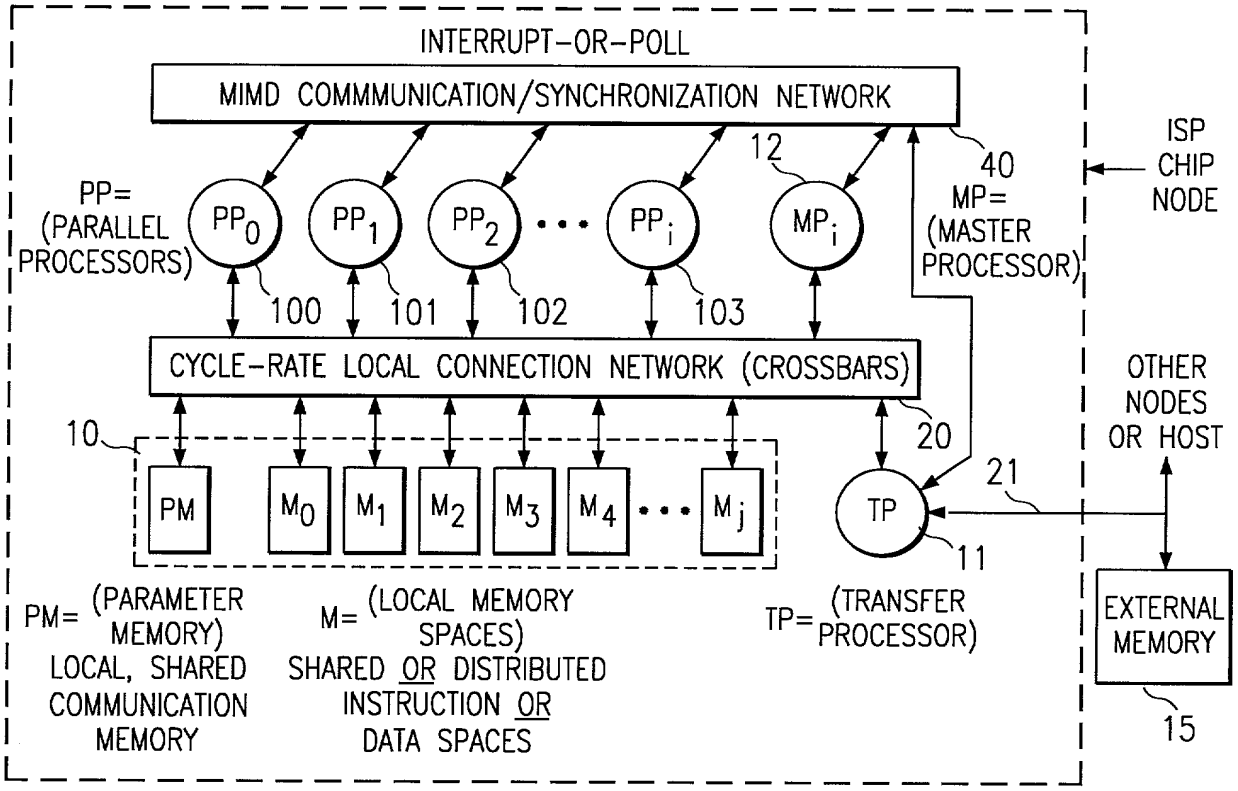

INTERRUPT-OR-POLL
MIMD COMMMUNICATION/SYNCHRONIZATION NETWORK
12
40
ISP CHIP NODE
PP= (PARALLEL PROCESSORS)
PP0
PP1
PP2
PPi
MPi
MP= (MASTER PROCESSOR)
100
101
102
103
CYCLE-RATE LOCAL CONNECTION NETWORK (CROSSBARS)
OTHER NODES OR HOST
10
20
21
PM
M0
M1
M2
M3
M4
Mj
TP
11
EXTERNAL MEMORY
15
PM= (PARAMETER MEMORY) LOCAL, SHARED COMMUNICATION MEMORY
M= (LOCAL MEMORY SPACES) SHARED OR DISTRIBUTED INSTRUCTION OR DATA SPACES
TP= (TRANSFER PROCESSOR)

FIG. 1

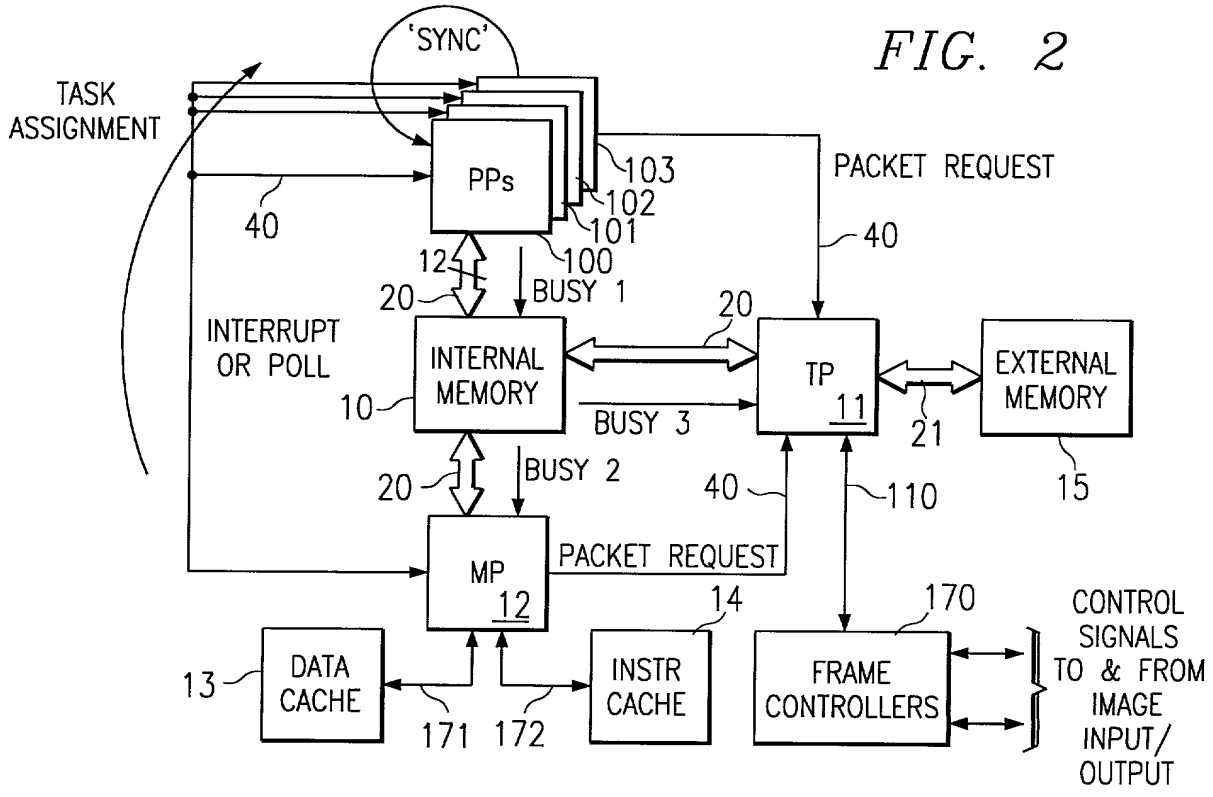

'SYNC'
TASK ASSIGNMENT
PPs
103
102
101
100
PACKET REQUEST
40
12
20
BUSY 1
INTERRUPT OR POLL
INTERNAL MEMORY
10
TP 11
BUSY 3
EXTERNAL MEMORY
21
15
BUSY 2
110
MP 12
PACKET REQUEST
14
170
13
DATA CACHE
171
172
INSTR CACHE
FRAME CONTROLLERS
CONTROL SIGNALS TO & FROM IMAGE INPUT/ OUTPUT

FIG. 2

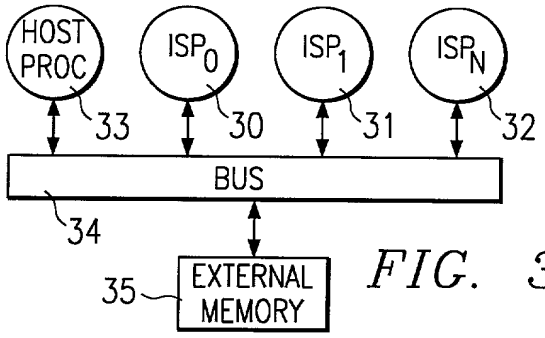


FIG. 3

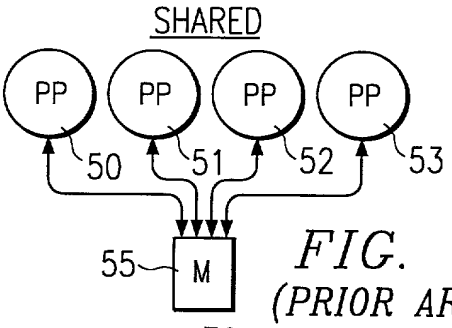


FIG. 5
(PRIOR ART)

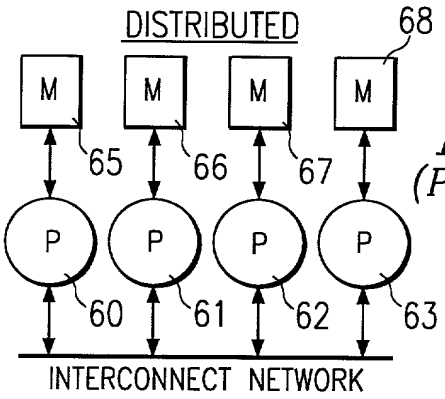


FIG. 6
(PRIOR ART)

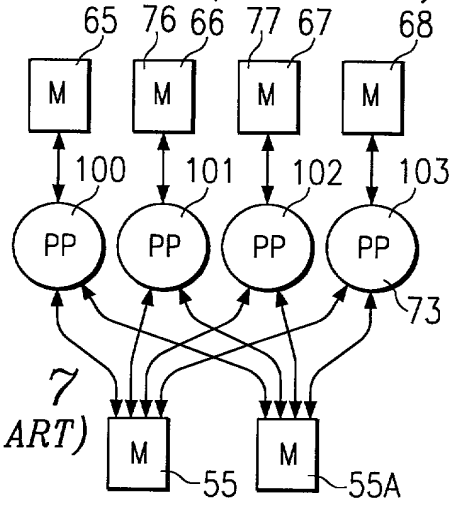


FIG. 7
(PRIOR ART)

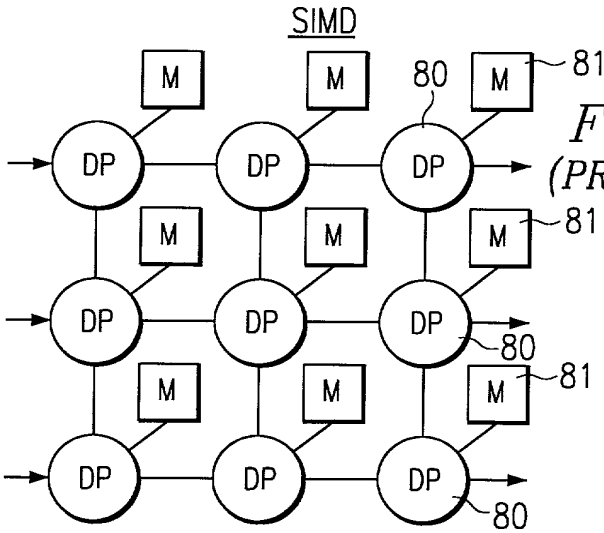


FIG. 8
(PRIOR ART)

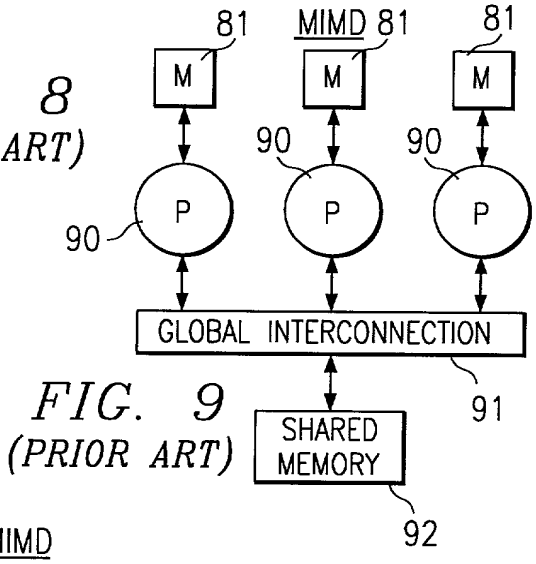


FIG. 9
(PRIOR ART)

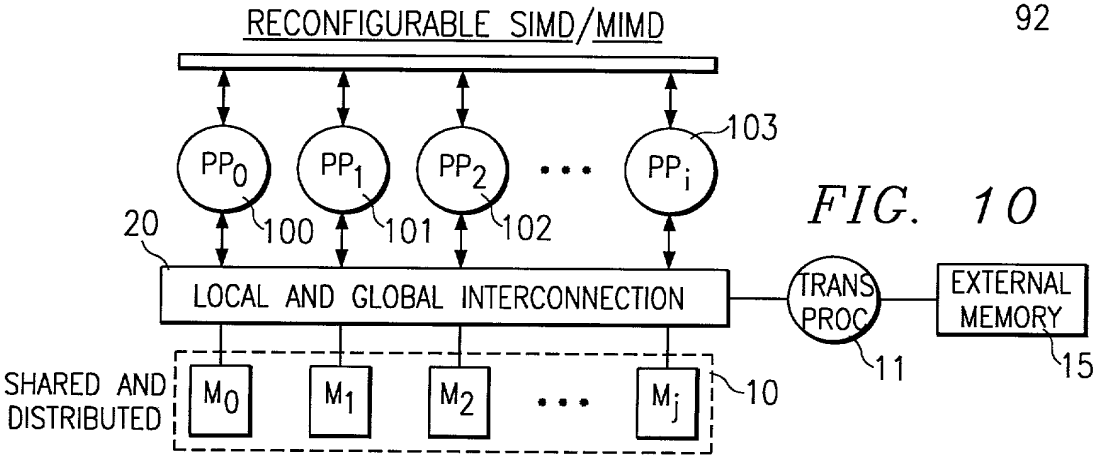


FIG. 10

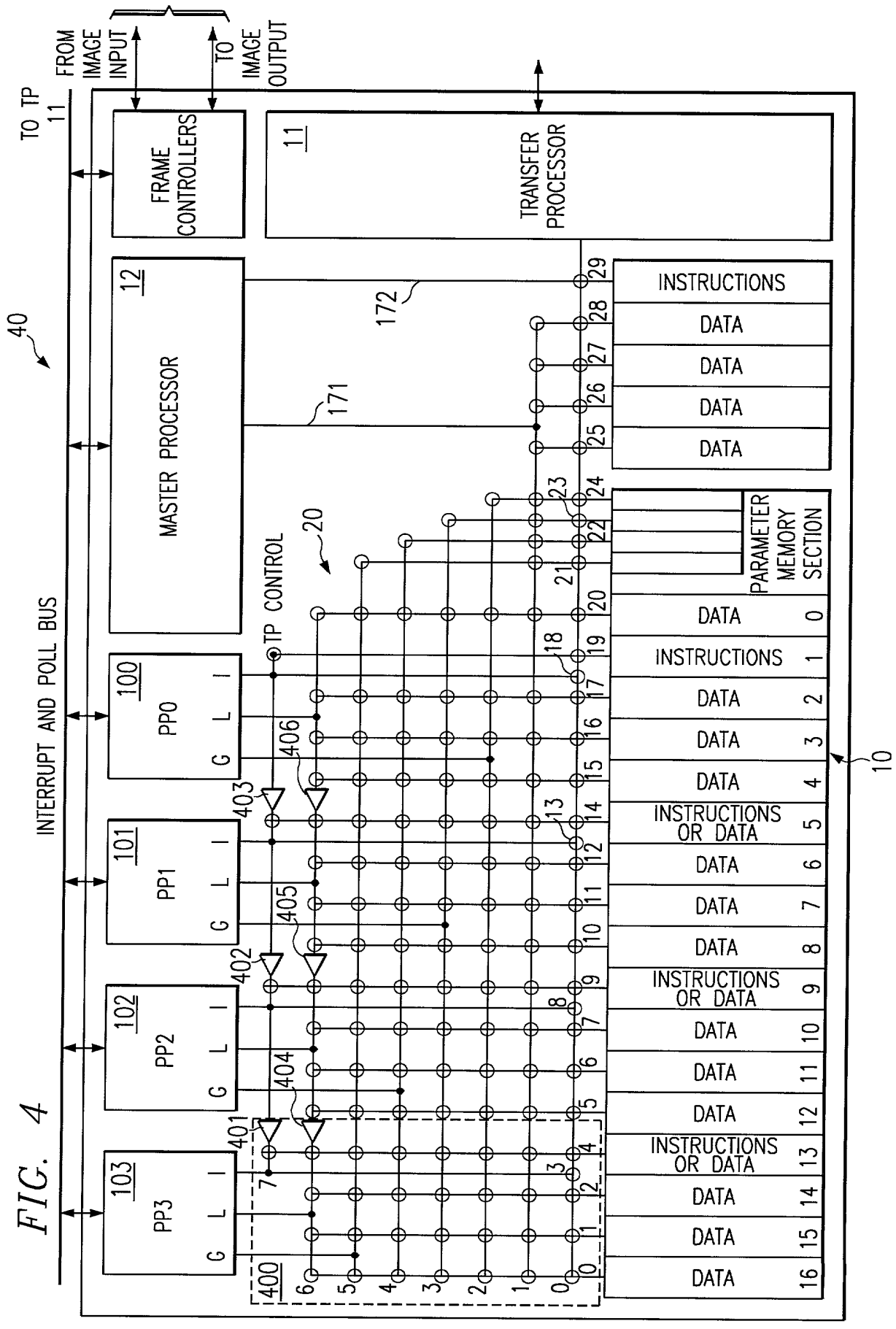


FIG. 4
40
TO TP 11
FROM IMAGE INPUT
TO IMAGE OUTPUT
FRAME CONTROLLERS
11
TRANSFER PROCESSOR
12
MASTER PROCESSOR
INTERRUPT AND POLL BUS
100
PP0
101
PP1
102
PP2
103
PP3
G L I
TP CONTROL
20
171
172
400
401
402
403
404
405
406
INSTRUCTIONS
DATA
INSTRUCTIONS OR DATA
PARAMETER MEMORY SECTION
10

FIG. 11

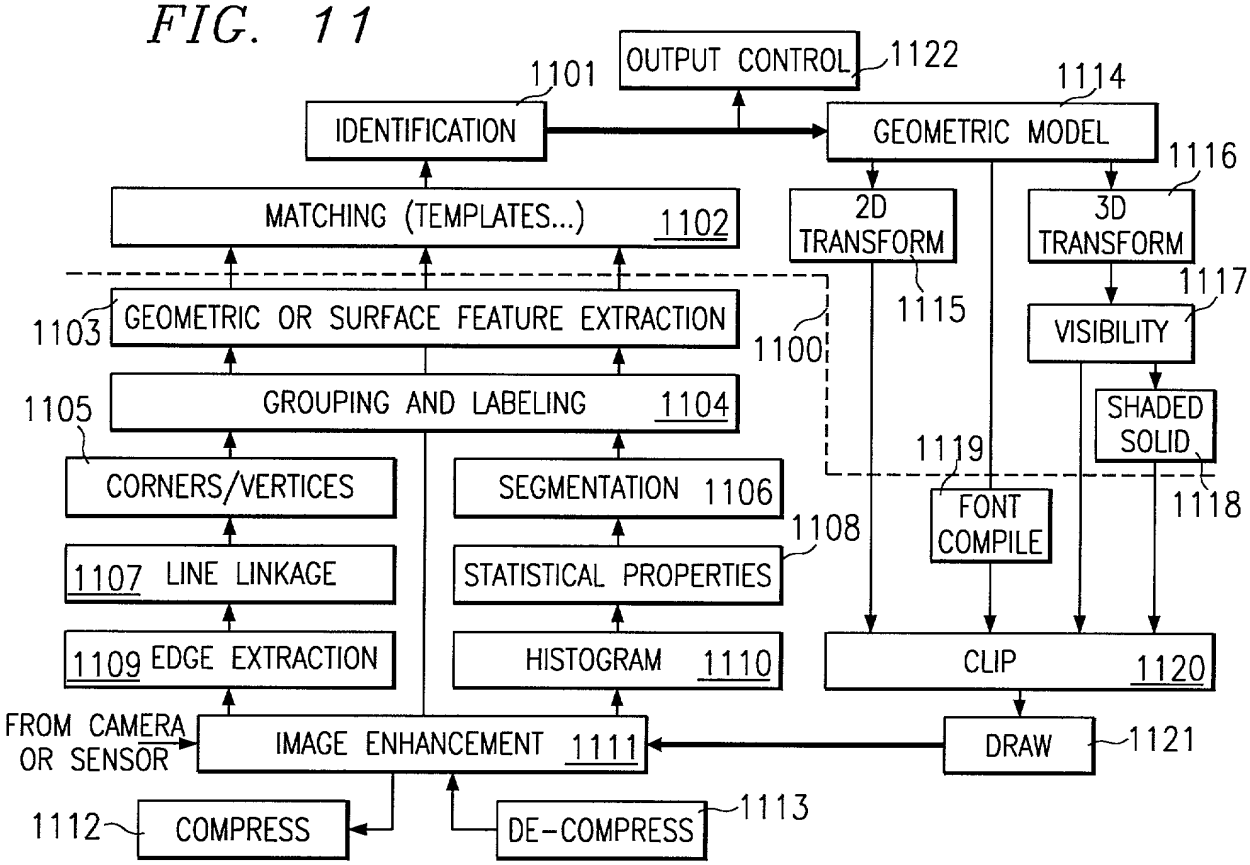

OUTPUT CONTROL
1122
1101
1114
IDENTIFICATION
GEOMETRIC MODEL
1116
MATCHING (TEMPLATES...) 1102
2D TRANSFORM
3D TRANSFORM
1115
1117
1103
GEOMETRIC OR SURFACE FEATURE EXTRACTION
1100
VISIBILITY
1105
GROUPING AND LABELING 1104
SHADED SOLID
1119
CORNERS/VERTICES
SEGMENTATION 1106
1118
FONT COMPILE
1108
1107 LINE LINKAGE
STATISTICAL PROPERTIES
1109 EDGE EXTRACTION
HISTOGRAM 1110
CLIP 1120
FROM CAMERA OR SENSOR
IMAGE ENHANCEMENT 1111
DRAW
1121
1112
COMPRESS
DE-COMPRESS
1113

FIG. 12

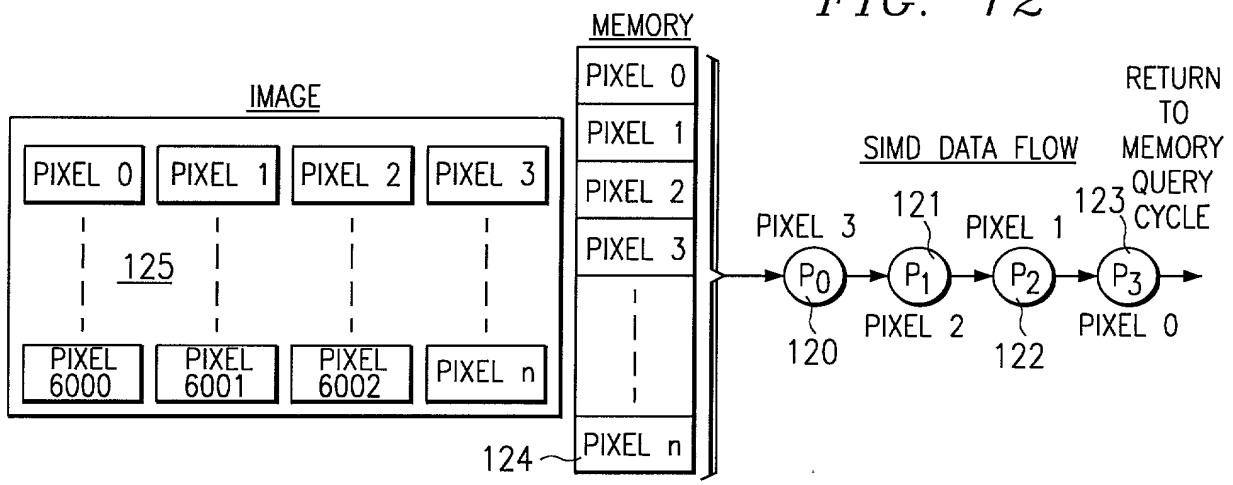

MEMORY
IMAGE
PIXEL 0
PIXEL 1
PIXEL 2
PIXEL 3
PIXEL n
125
PIXEL 6000
PIXEL 6001
PIXEL 6002
124
SIMD DATA FLOW
RETURN TO MEMORY QUERY CYCLE
121
123
PIXEL 3
PIXEL 1
P0
P1
P2
P3
PIXEL 2
PIXEL 0
120
122

FIG. 13

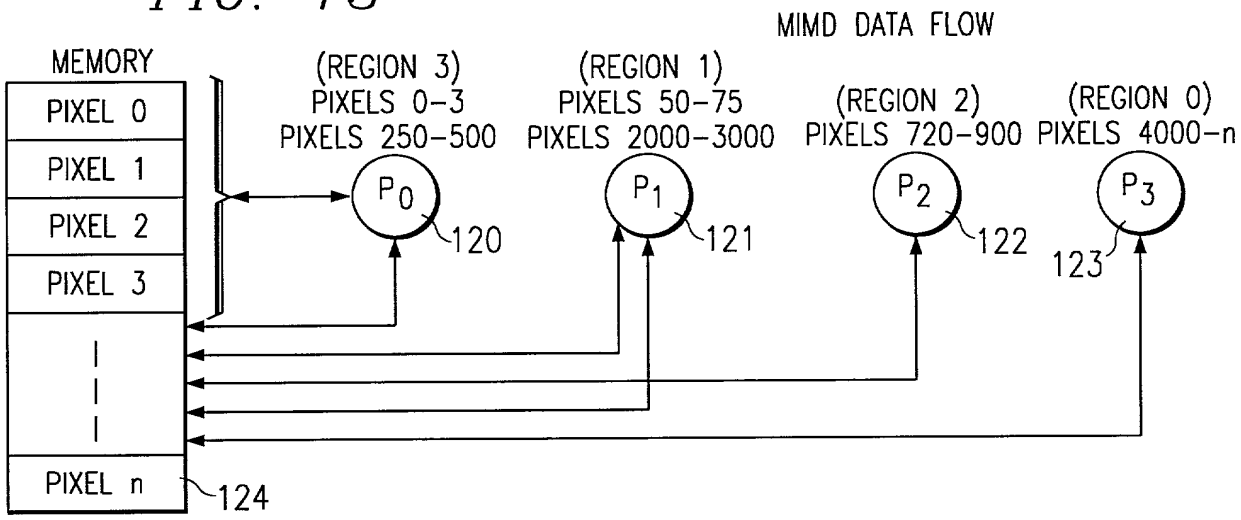


FIG. 14

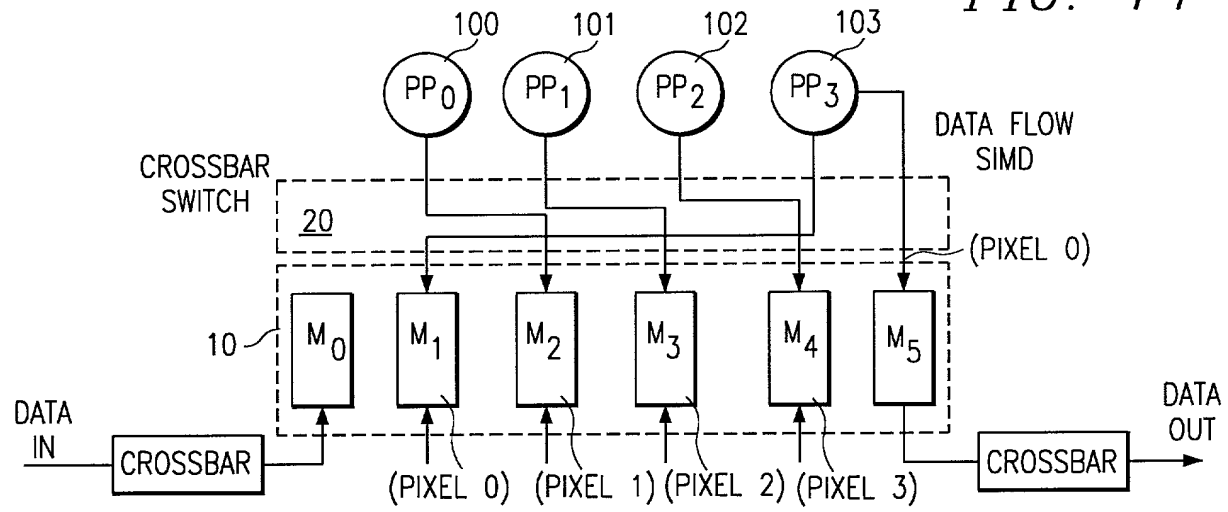


FIG. 15

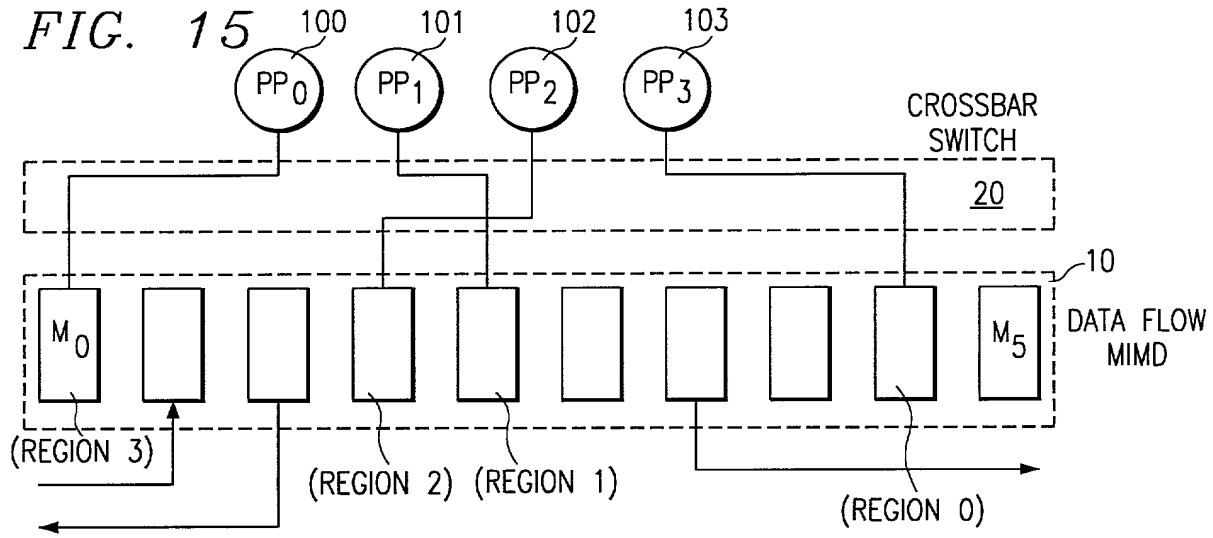
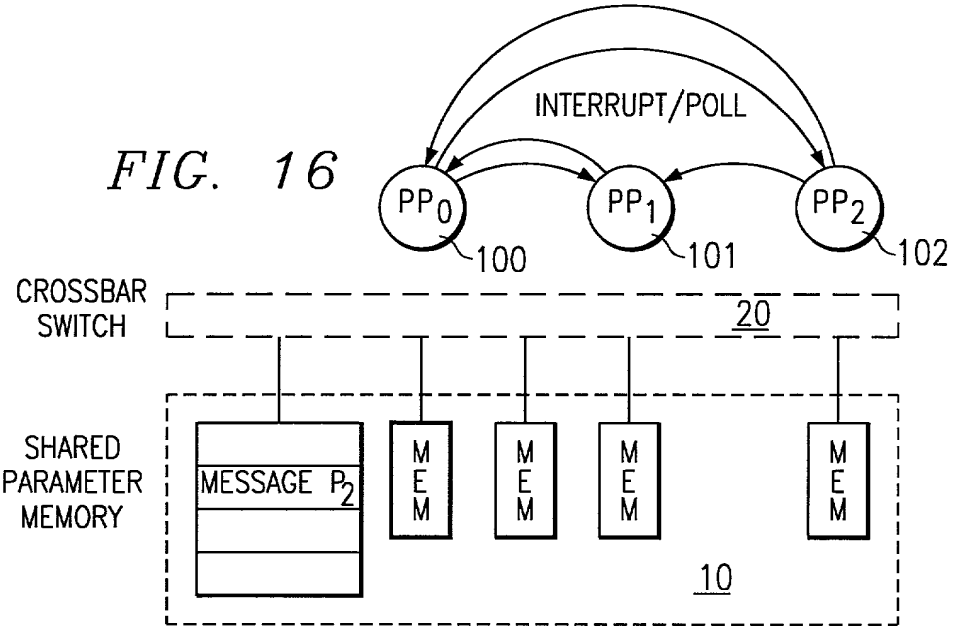


FIG. 16


INTERRUPT/POLL
PP0
PP1
PP2
100
101
102
CROSSBAR SWITCH
20
SHARED PARAMETER MEMORY
MESSAGE P2
MEM
MEM
MEM
MEM
10

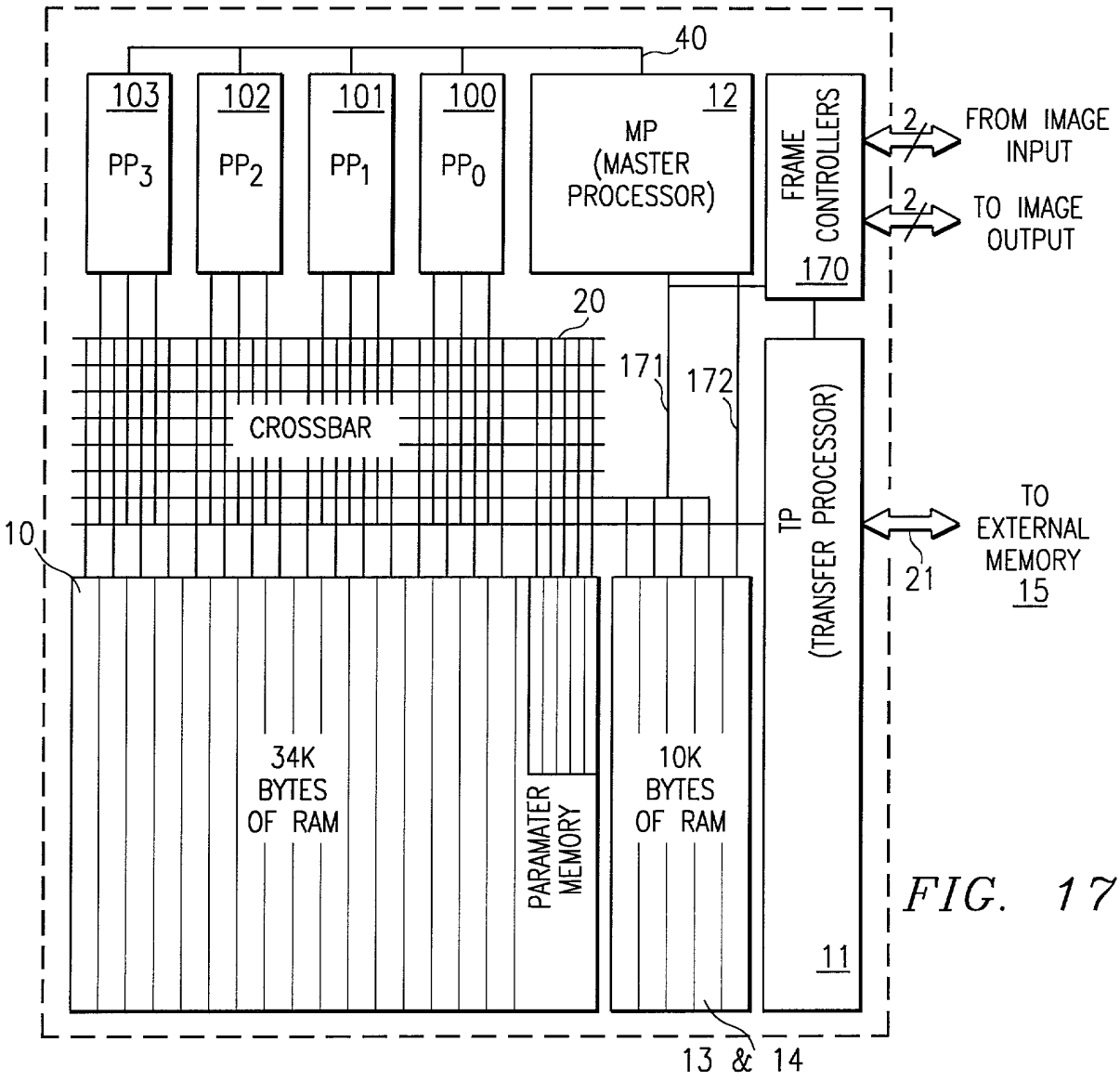

40
103
PP3
102
PP2
101
PP1
100
PP0
12
MP (MASTER PROCESSOR)
FRAME CONTROLLERS
170
2
FROM IMAGE INPUT
2
TO IMAGE OUTPUT
20
171
172
CROSSBAR
10
TP (TRANSFER PROCESSOR)
TO EXTERNAL MEMORY
15
21
34K BYTES OF RAM
PARAMATER MEMORY
10K BYTES OF RAM
11
13 & 14

FIG. 17

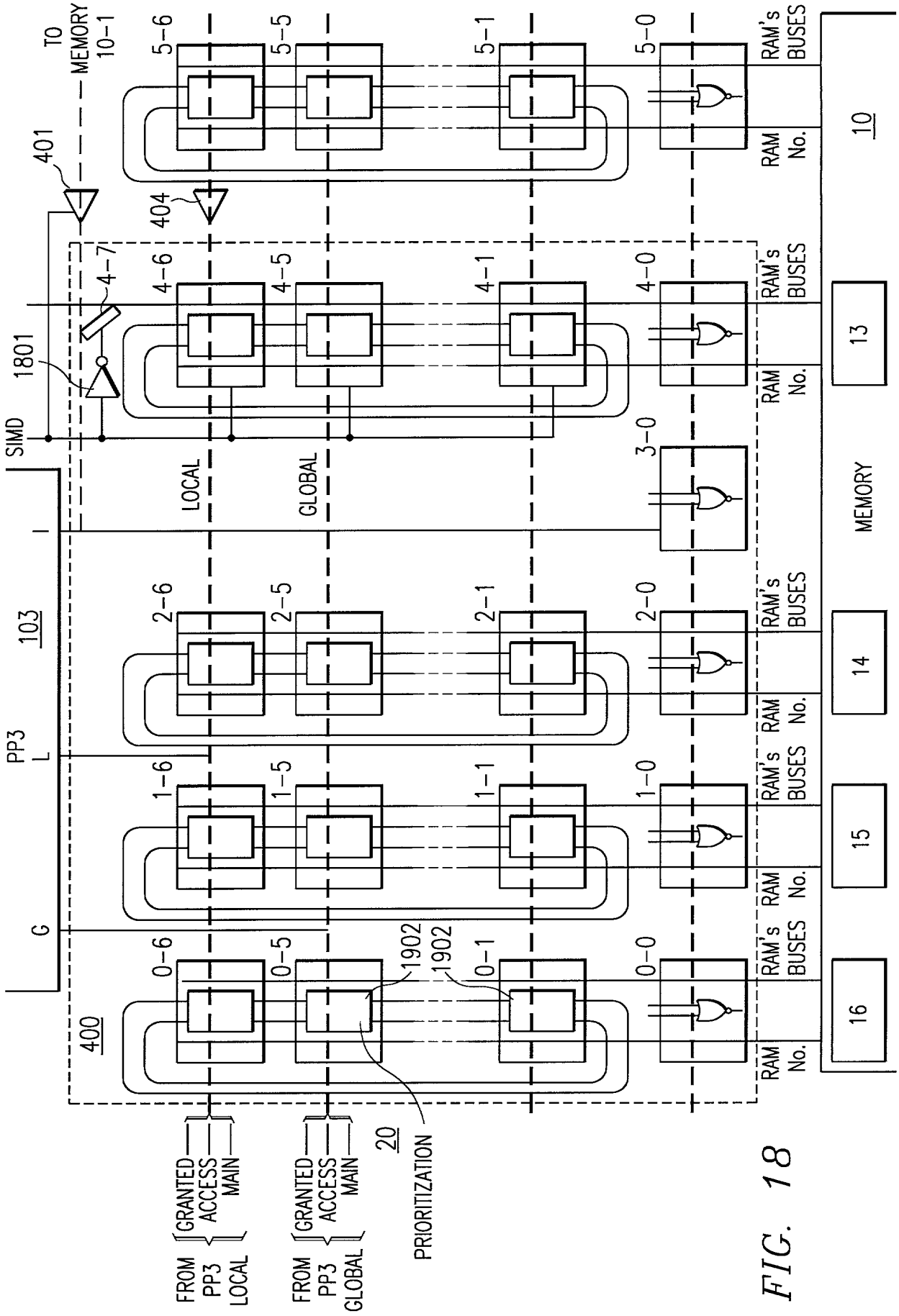

TO MEMORY 10-1
401
404
SIMD
1801
4-7
LOCAL
GLOBAL
PP3 103
L
I
G
400
5-6
5-5
5-1
5-0
4-6
4-5
4-1
4-0
3-0
2-6
2-5
2-1
2-0
1-6
1-5
1-1
1-0
0-6
0-5
0-1
0-0
1902
1902
RAM's BUSES
RAM No.
10
MEMORY
13
14
15
16
20
PRIORITIZATION
FROM PP3 LOCAL
GRANTED ACCESS MAIN
FROM PP3 GLOBAL
GRANTED ACCESS MAIN

FIG. 18

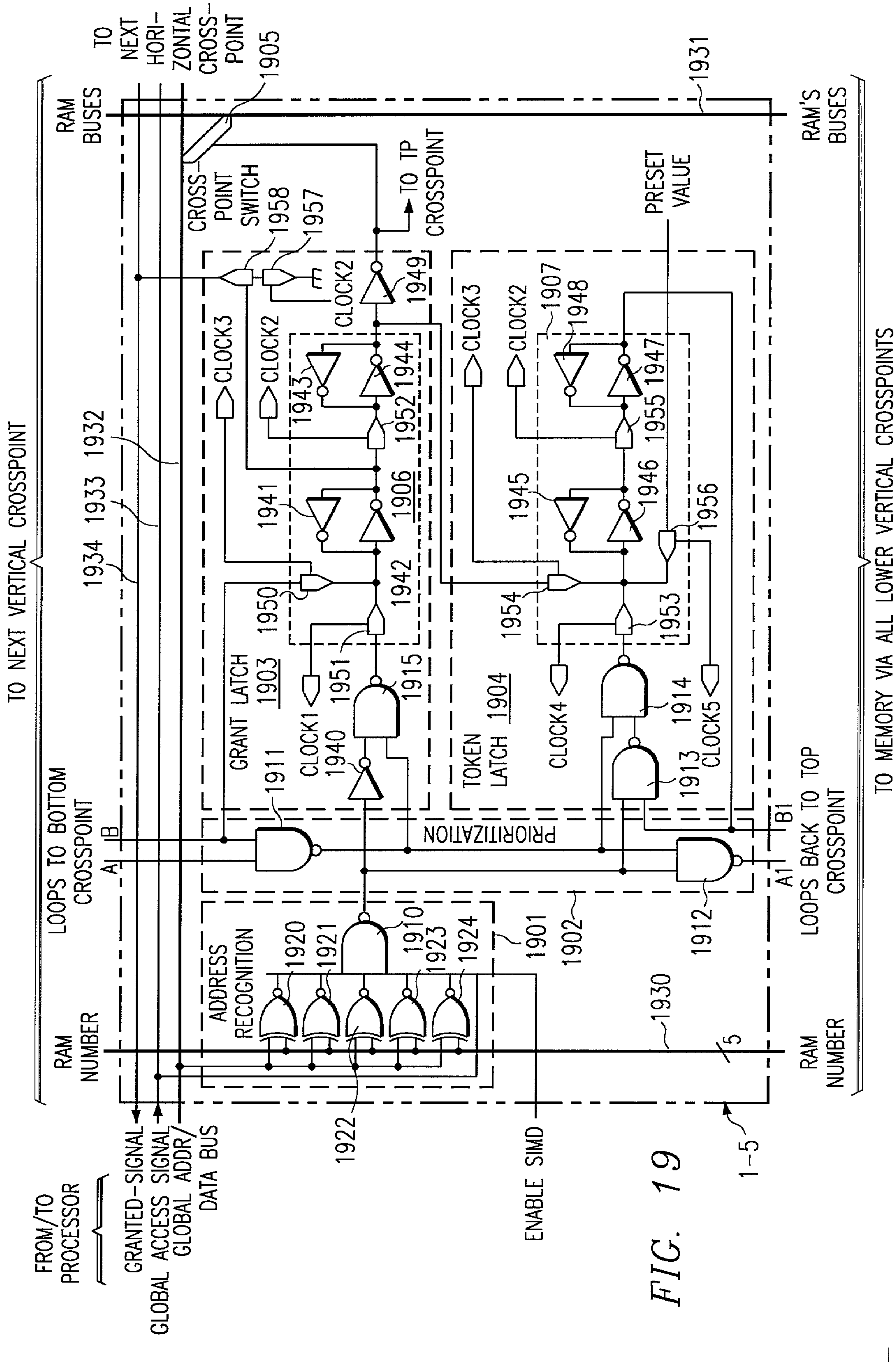
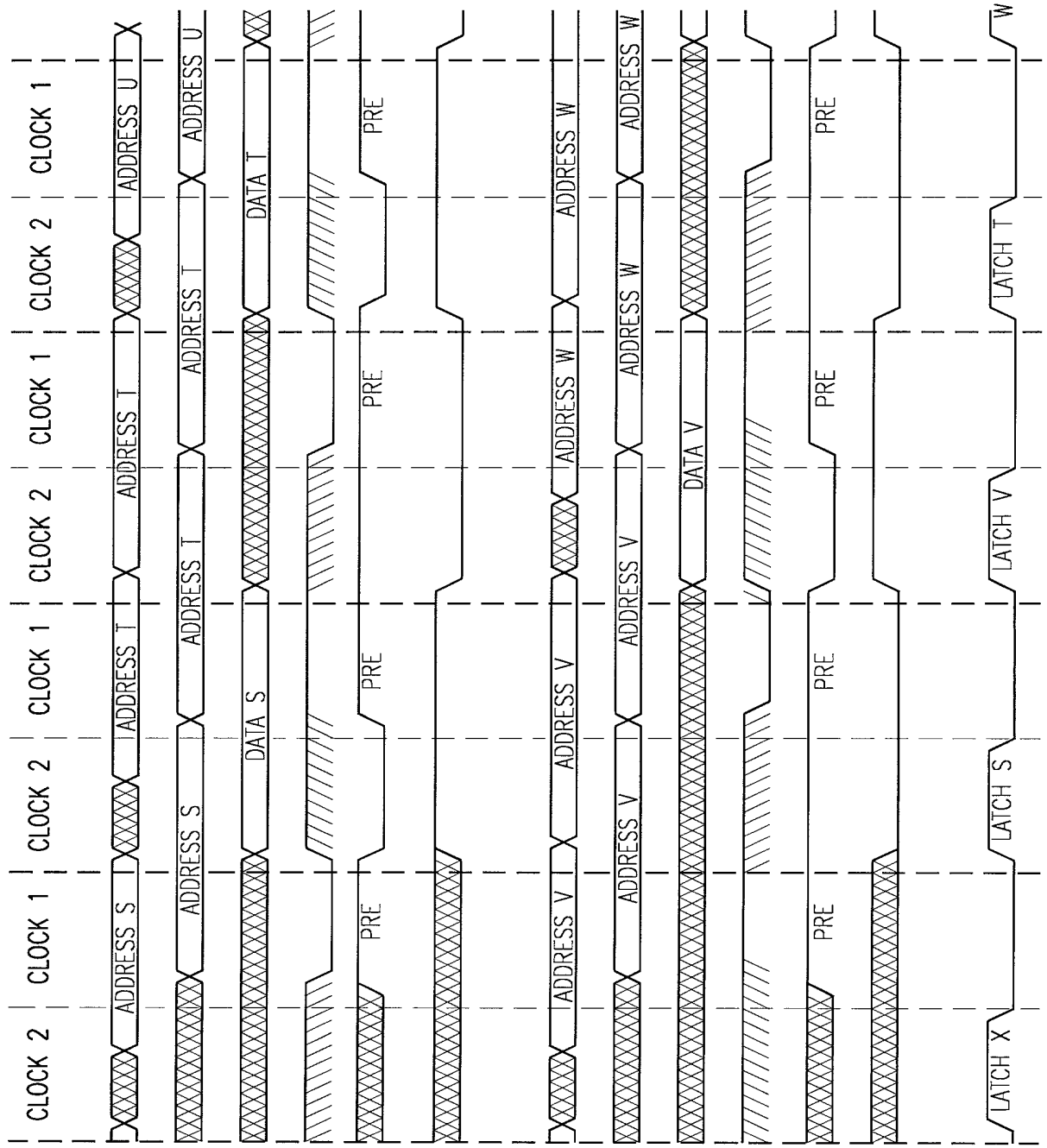

TO NEXT VERTICAL CROSSPOINT
TO NEXT HORIZONTAL CROSSPOINT
RAM BUSES
RAM'S BUSES
RAM NUMBER
CROSSPOINT SWITCH
TO TP CROSSPOINT
PRESET VALUE
GRANT LATCH 1903
TOKEN LATCH 1904
ADDRESS RECOGNITION
PRIORITIZATION
LOOPS TO BOTTOM CROSSPOINT
LOOPS BACK TO TOP CROSSPOINT
A
B
A1
B1
CLOCK1
CLOCK2
CLOCK3
CLOCK4
CLOCK5
FROM/TO PROCESSOR
GRANTED-SIGNAL
GLOBAL ACCESS SIGNAL
GLOBAL ADDR/DATA BUS
ENABLE SIMD
TO MEMORY VIA ALL LOWER VERTICAL CROSSPOINTS
1-5
5
1901
1902
1905
1906
1907
1910
1911
1912
1913
1914
1915
1920
1921
1922
1923
1924
1930
1931
1932
1933
1934
1940
1941
1942
1943
1944
1945
1946
1947
1948
1949
1950
1951
1952
1953
1954
1955
1956
1957
1958

FIG. 19

FIG. 20



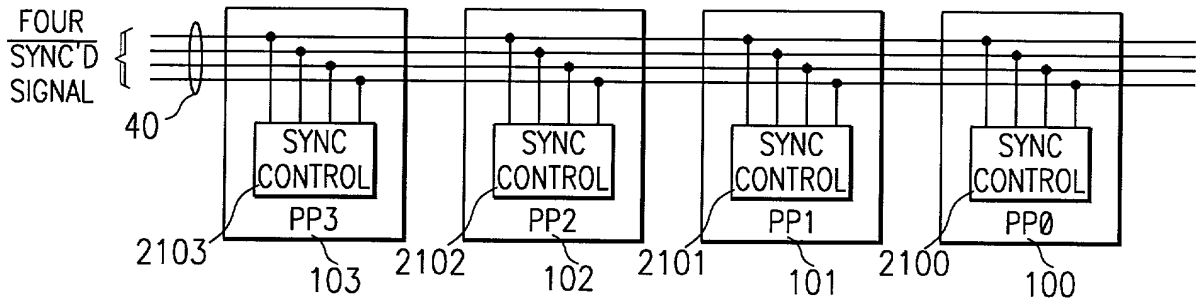


FIG. 21

>0000	>0800	>1000	>1800	>2000	>2800	>3000	>3800
64 PIXELS	64 PIXELS	64 PIXELS	>1900 >193F	>2100 >213F	64 PIXELS	64 PIXELS	64 PIXELS
>07FF	>0FFF	>17FF	>1940 >1FFF	>27FF	>2FFF	>37FF	>3FFF
0	1	2	3	4	5	6	7

NORMAL ARITHMETIC

```
>193F  -  0 0 0 1 1 0 0 1 0 0 1 1 1 1 1 1
  +
>0001  -  0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1
  =
>1940  -  0 0 0 1 1 0 0 1 0 1 0 0 0 0 0 0
```

SLICED ARITHMETIC

```
                      SLICE NUMBER
>193F  -  0 0 0 1 1 0 0 1 0 0 1 1 1 1 1 1
(SLICE MASK)  0 0 0 0 0 1 1 1 1 1 0 0 0 0 0 0
                        CARRY
  +
>0001  -  0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1
  =
>2100  -  0 0 1 0 0 0 0 1 0 0 0 0 0 0 0 0
```

FIG. 27

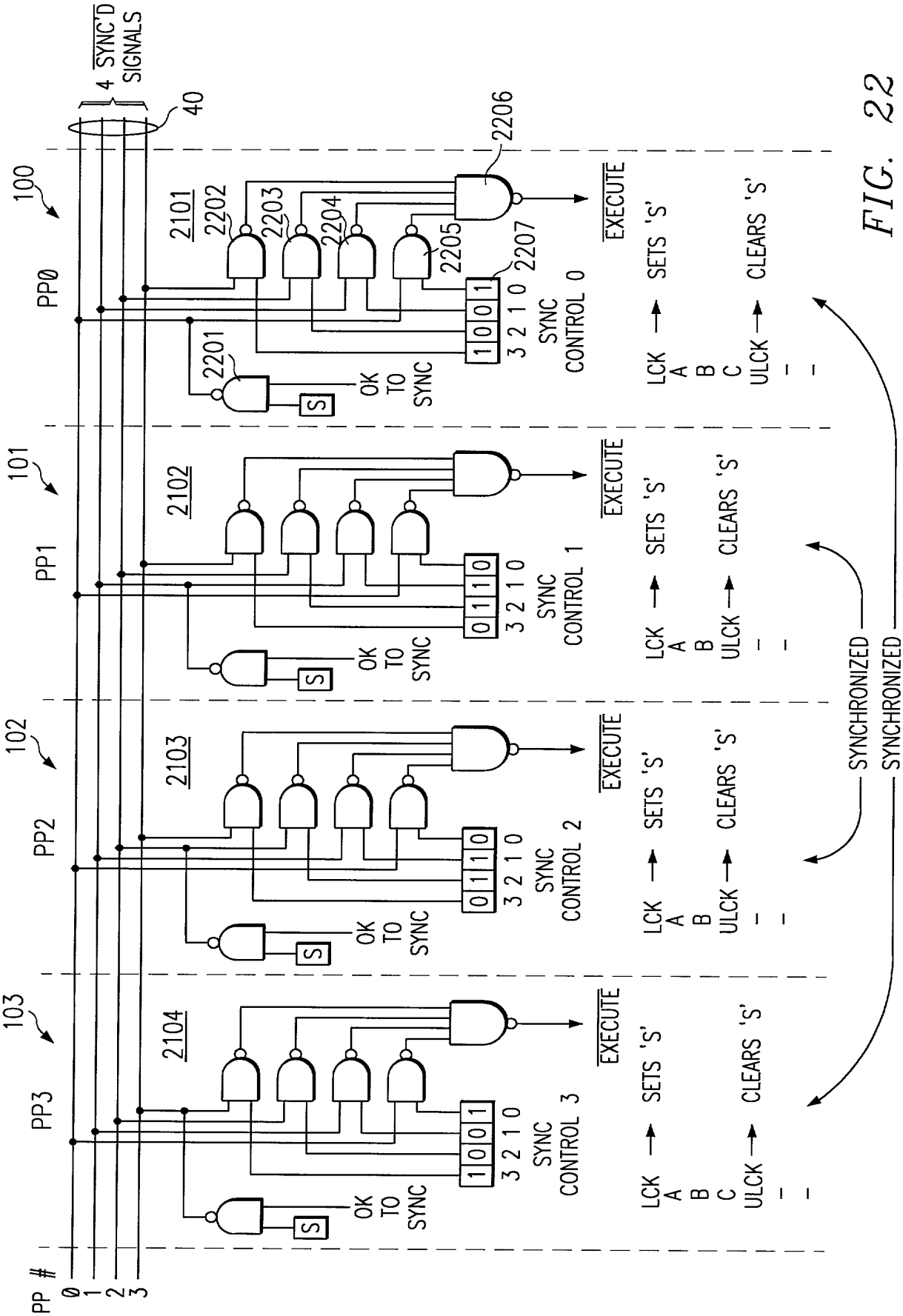

PP #
0
1
2
3
4 SYNC'D SIGNALS
40
100
PP0
101
PP1
102
PP2
103
PP3
2101
2102
2103
2104
2201
2202
2203
2204
2205
2206
2207
S
OK TO SYNC
3 2 1 0
SYNC CONTROL 0
SYNC CONTROL 1
SYNC CONTROL 2
SYNC CONTROL 3
1 0 0 1
0 1 1 0
EXECUTE
LCK → SETS 'S'
A
B
ULCK → CLEARS 'S'
C
SYNCHRONIZED
SYNCHRONIZED

FIG. 22

(3210)
SYNC BITS = 0110
IN BOTH PP2 AND PP1

	PP2:	PP1:
	–	–
0	LCK	LCK
1	ST *A0,D0	ST *A1,D0
2	LD *A1,D0	LD *A0,D0
3	ULCK	ULCK
4	–	–
5	–	–

FIG. 23

m – MASTER CLOCK
s – SLAVE CLOCK

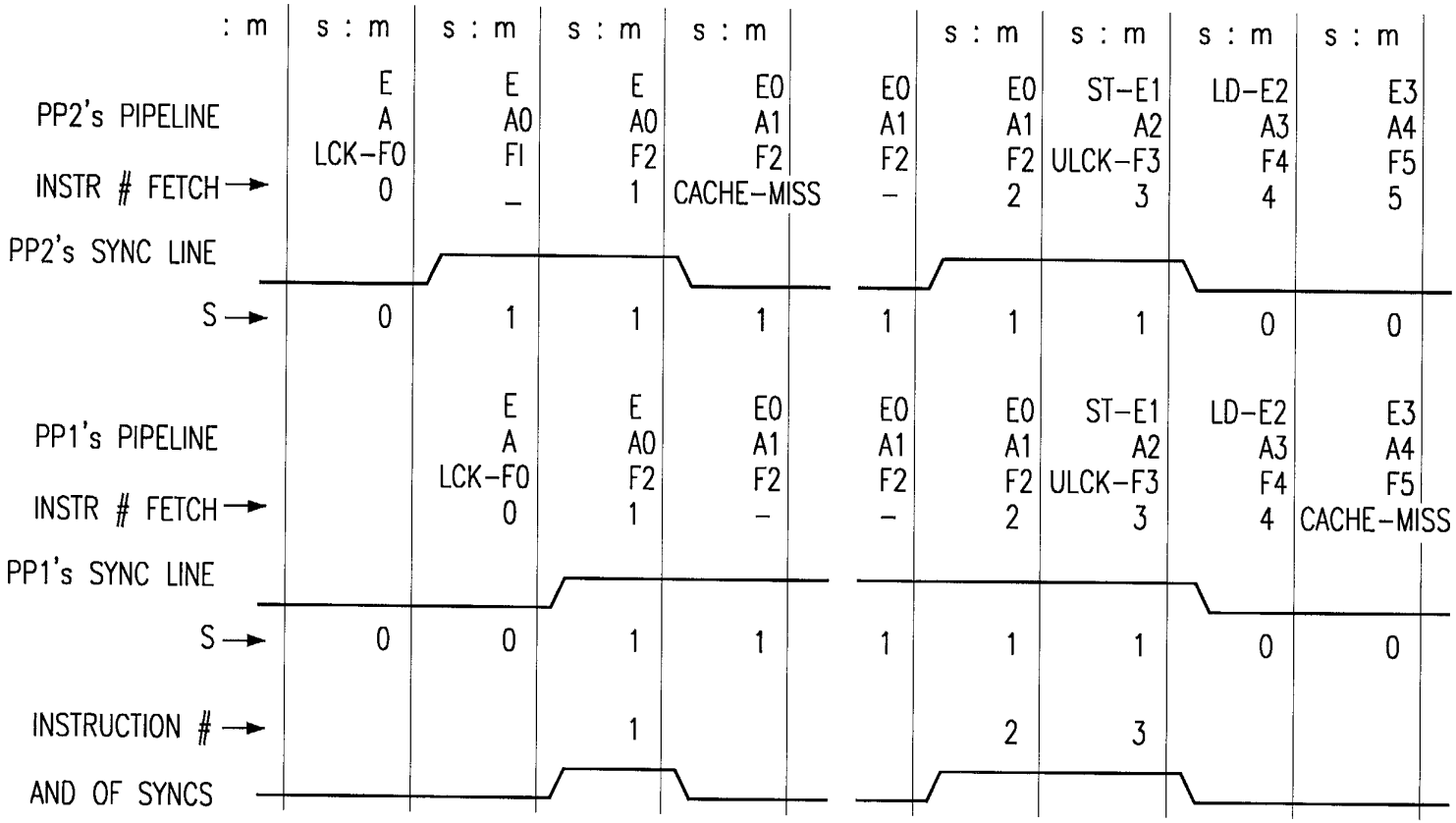


FIG. 24

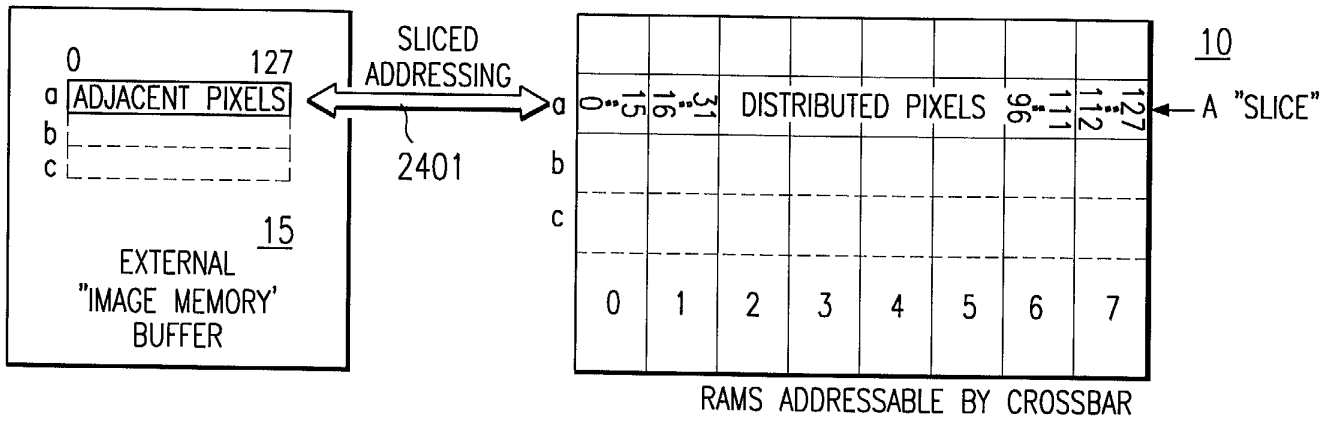


FIG. 25
(PRIOR ART)

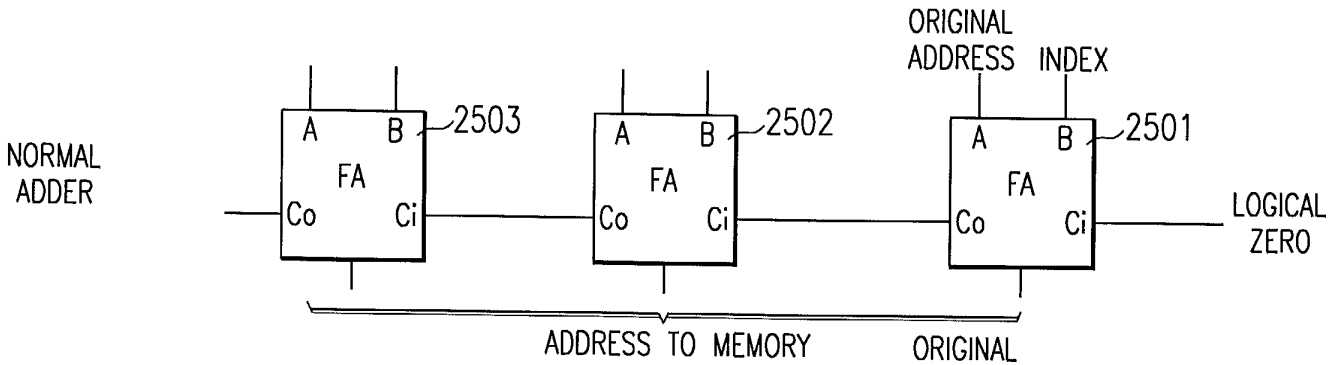
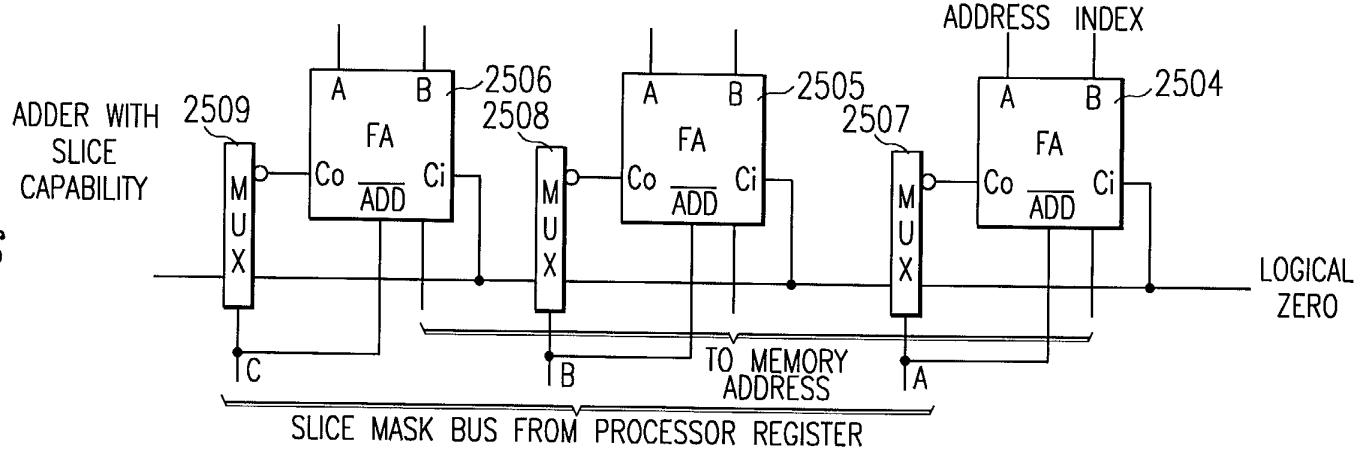


FIG. 26



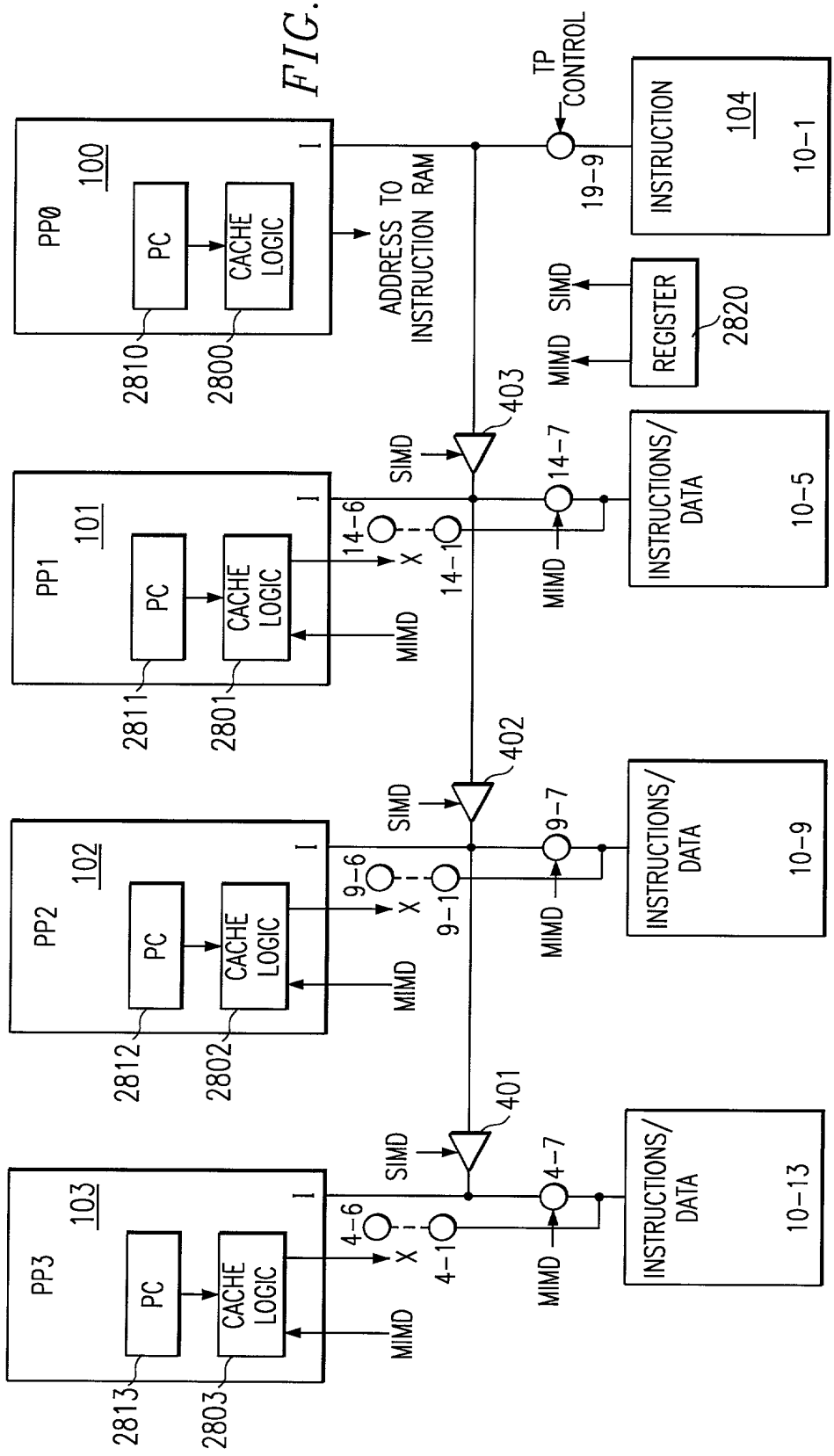
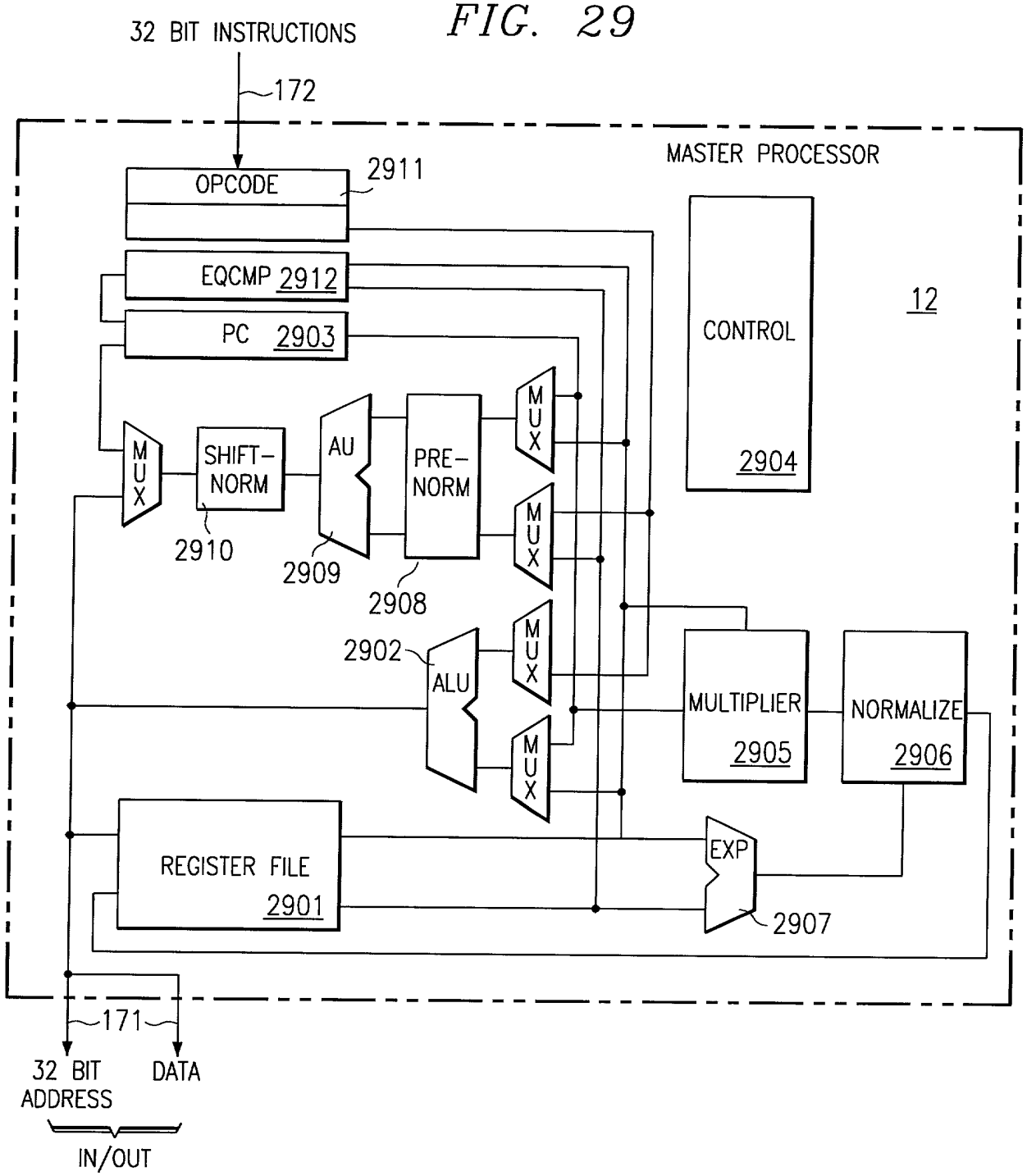

PP0
100
PC
CACHE LOGIC
2810
2800
ADDRESS TO INSTRUCTION RAM
TP CONTROL
19-9
INSTRUCTION
104
10-1
PP1
101
2811
2801
SIMD
403
MIMD
14-6
14-1
X
14-7
INSTRUCTIONS/ DATA
10-5
REGISTER
2820
PP2
102
2812
2802
402
9-6
9-1
9-7
10-9
PP3
103
2813
2803
401
4-6
4-1
4-7
10-13

FIG. 28

FIG. 29


32 BIT INSTRUCTIONS
172
MASTER PROCESSOR
OPCODE
2911
EQCMP 2912
PC 2903
CONTROL
2904
12
MUX
SHIFT–NORM
2910
AU
2909
PRE–NORM
2908
MUX
MUX
MUX
2902
ALU
MUX
MULTIPLIER
2905
NORMALIZE
2906
REGISTER FILE
2901
EXP
2907
171
32 BIT ADDRESS
DATA
IN/OUT

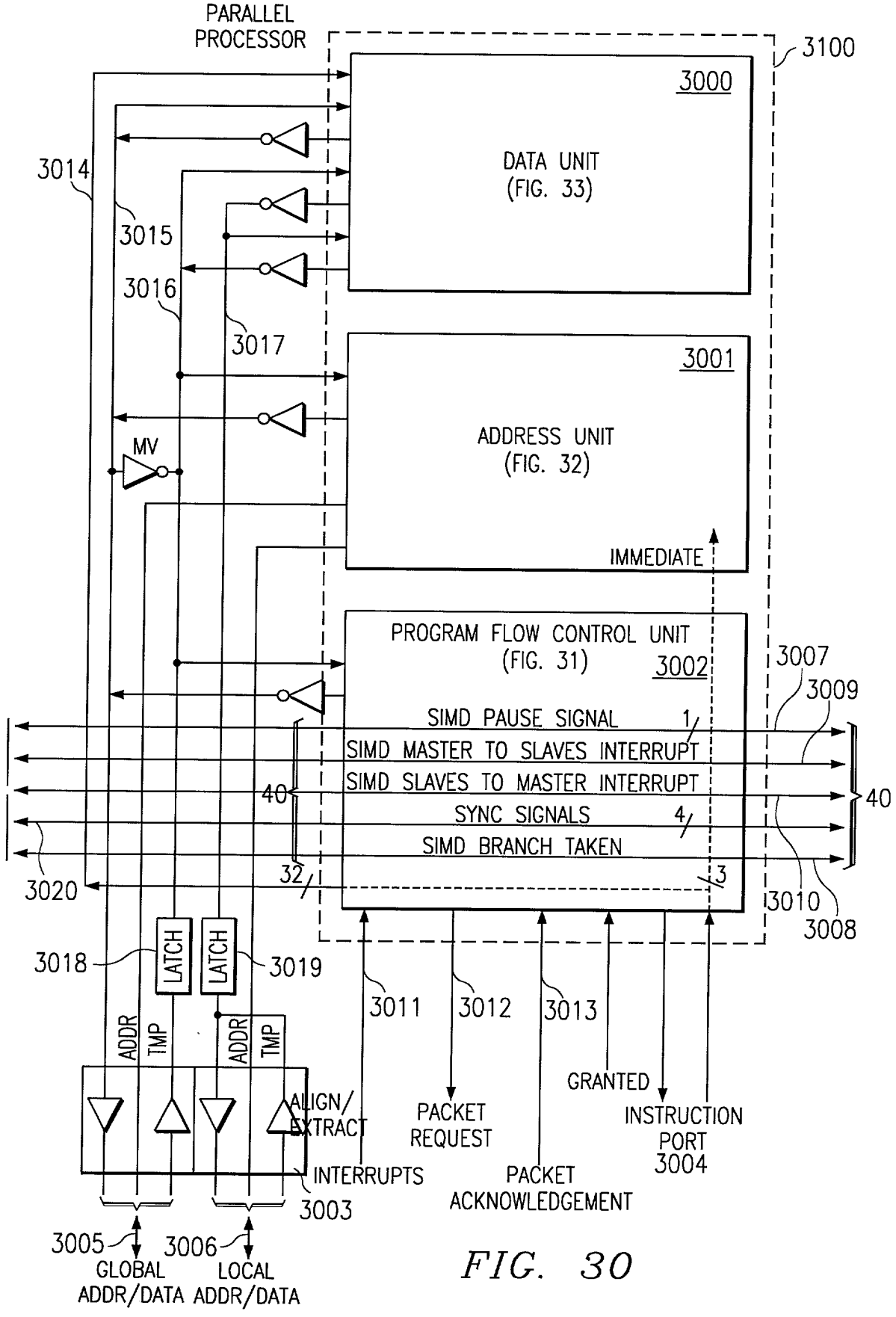

PARALLEL PROCESSOR
3100
3000
DATA UNIT (FIG. 33)
3014
3015
3016
3017
3001
ADDRESS UNIT (FIG. 32)
MV
IMMEDIATE
PROGRAM FLOW CONTROL UNIT (FIG. 31)
3002
3007
3009
SIMD PAUSE SIGNAL
SIMD MASTER TO SLAVES INTERRUPT
SIMD SLAVES TO MASTER INTERRUPT
SYNC SIGNALS
SIMD BRANCH TAKEN
40
40
1
4
32
3
3020
3010
3008
3018
LATCH
LATCH
3019
ADDR
TMP
ADDR
TMP
3011
3012
3013
ALIGN/ EXTRACT
PACKET REQUEST
GRANTED
INSTRUCTION PORT 3004
INTERRUPTS
PACKET ACKNOWLEDGEMENT
3003
3005
3006
GLOBAL ADDR/DATA
LOCAL ADDR/DATA

FIG. 30

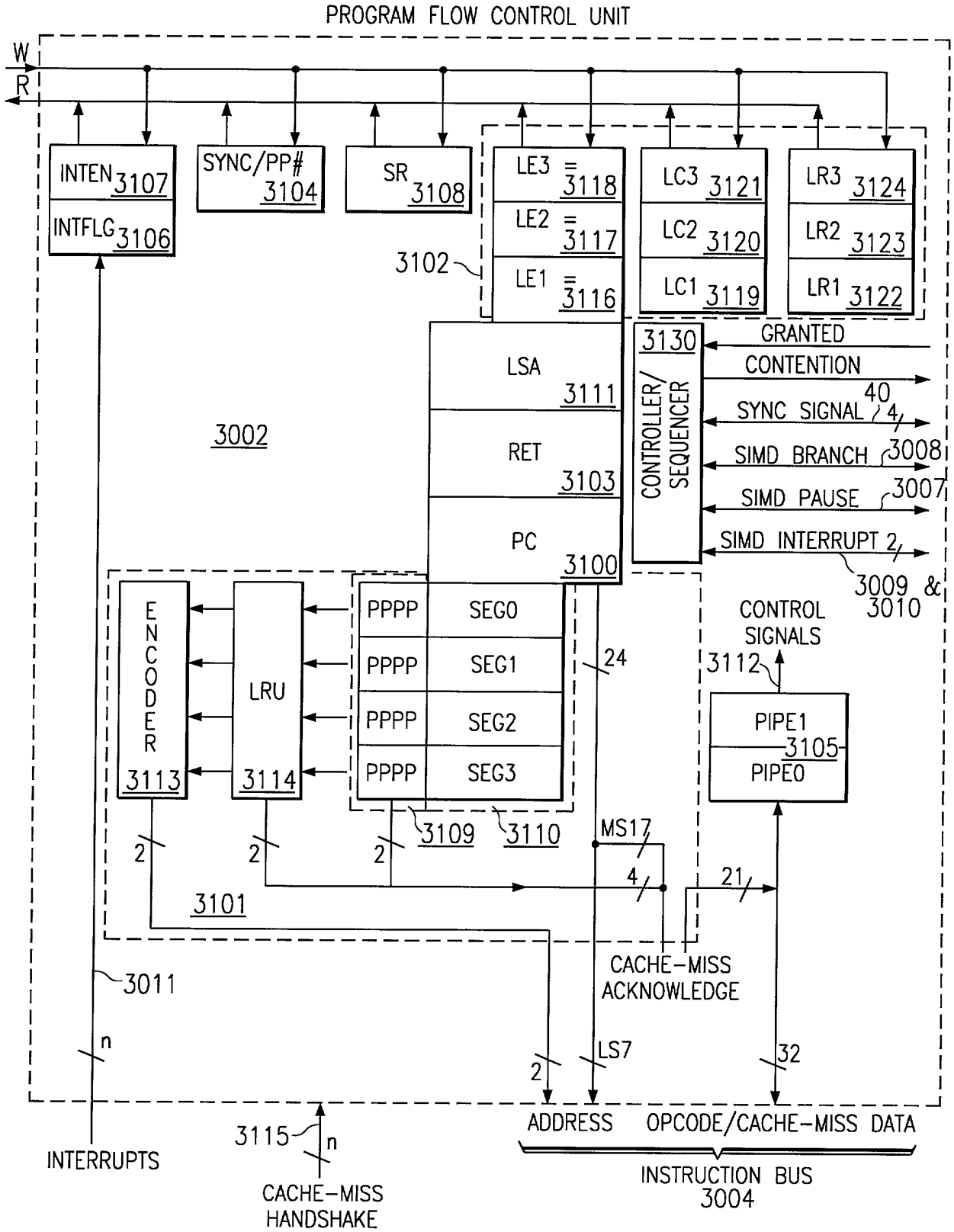

PROGRAM FLOW CONTROL UNIT
W
R
INTEN 3107
INTFLG 3106
SYNC/PP# 3104
SR 3108
LE3 3118
LE2 3117
LE1 3116
LC3 3121
LC2 3120
LC1 3119
LR3 3124
LR2 3123
LR1 3122
3102
LSA 3111
RET 3103
PC 3100
3002
3130
CONTROLLER/ SEQUENCER
GRANTED
CONTENTION
40
SYNC SIGNAL 4
SIMD BRANCH 3008
SIMD PAUSE 3007
SIMD INTERRUPT 2
3009 & 3010
CONTROL SIGNALS
3112
ENCODER 3113
LRU 3114
PPPP SEG0
PPPP SEG1
PPPP SEG2
PPPP SEG3
24
3109
3110
MS17
4
21
2
2
2
3101
PIPE1 3105
PIPE0
CACHE-MISS ACKNOWLEDGE
3011
n
2
LS7
32
3115
n
INTERRUPTS
CACHE-MISS HANDSHAKE
ADDRESS
OPCODE/CACHE-MISS DATA
INSTRUCTION BUS 3004

FIG. 31

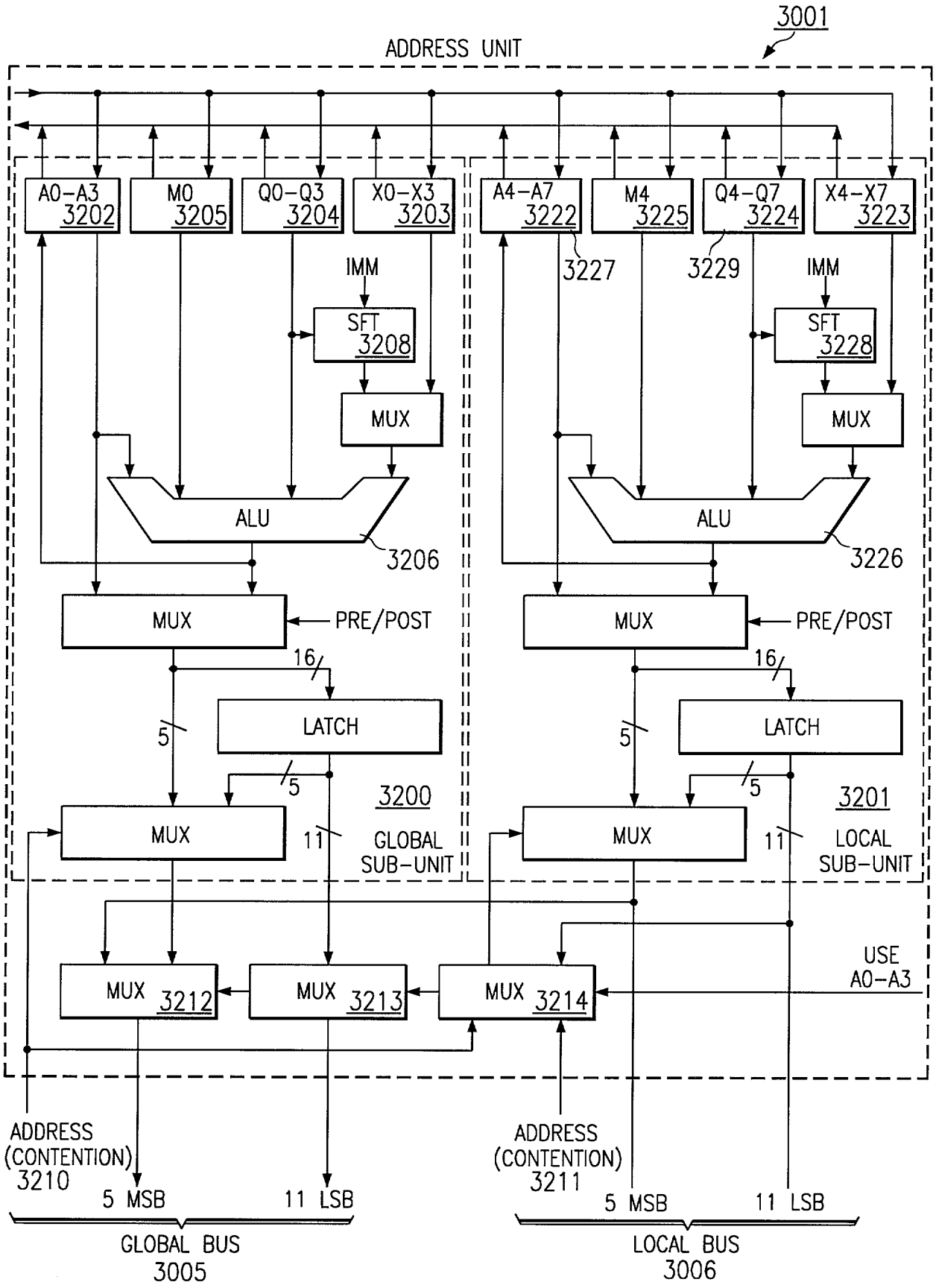

3001
ADDRESS UNIT
A0–A3
3202
M0
3205
Q0–Q3
3204
X0–X3
3203
A4–A7
3222
M4
3225
Q4–Q7
3224
X4–X7
3223
IMM
SFT
3208
MUX
ALU
3206
3227
3229
IMM
SFT
3228
MUX
ALU
3226
MUX
PRE/POST
16
5
LATCH
5
3200
MUX
11
GLOBAL
SUB–UNIT
MUX
PRE/POST
16
5
LATCH
5
3201
MUX
11
LOCAL
SUB–UNIT
MUX
3212
MUX
3213
MUX
3214
USE
A0–A3
ADDRESS
(CONTENTION)
3210
5 MSB
11 LSB
GLOBAL BUS
3005
ADDRESS
(CONTENTION)
3211
5 MSB
11 LSB
LOCAL BUS
3006

FIG. 32

FIG. 33

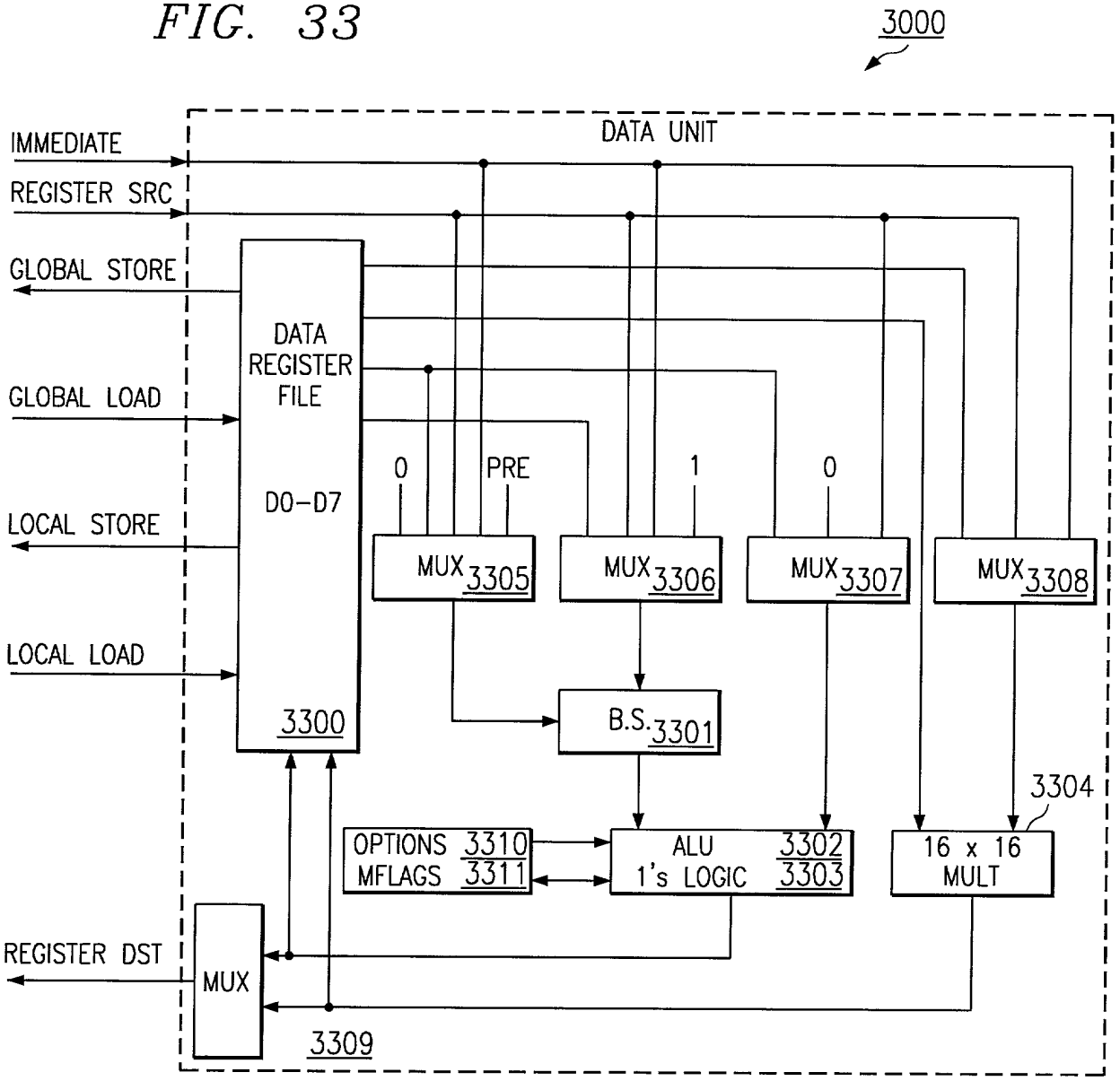

3000
DATA UNIT
IMMEDIATE
REGISTER SRC
GLOBAL STORE
GLOBAL LOAD
LOCAL STORE
LOCAL LOAD
REGISTER DST
DATA REGISTER FILE
D0–D7
3300
0
PRE
1
0
MUX 3305
MUX 3306
MUX 3307
MUX 3308
B.S. 3301
3304
OPTIONS 3310
MFLAGS 3311
ALU 3302
1's LOGIC 3303
16 x 16 MULT
MUX
3309

FIG. 34

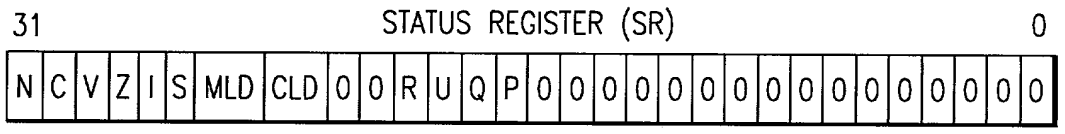
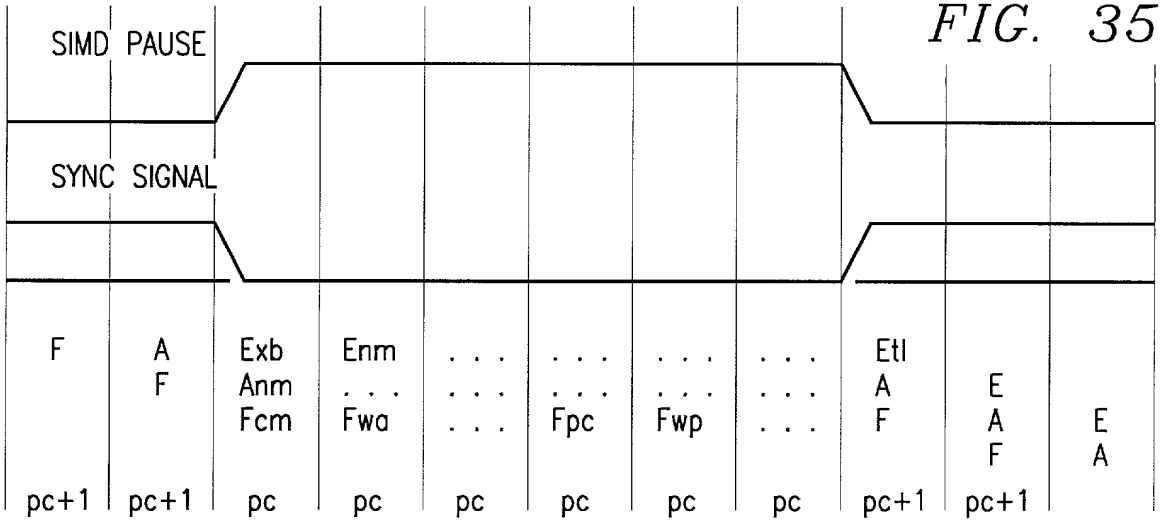
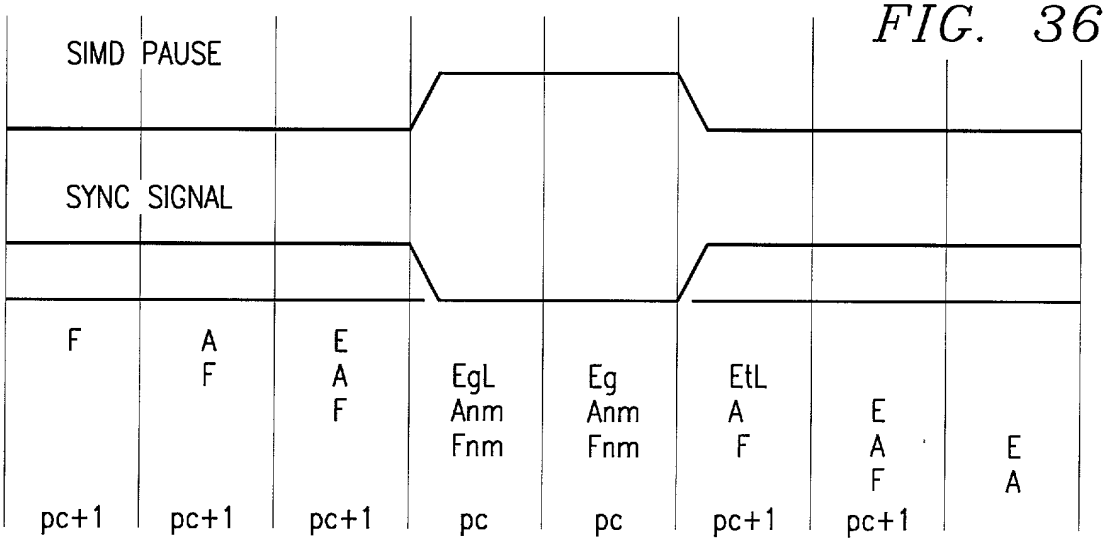

31
STATUS REGISTER (SR)
0
N C V Z I S MLD CLD 0 0 R U Q P 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

FIG. 35

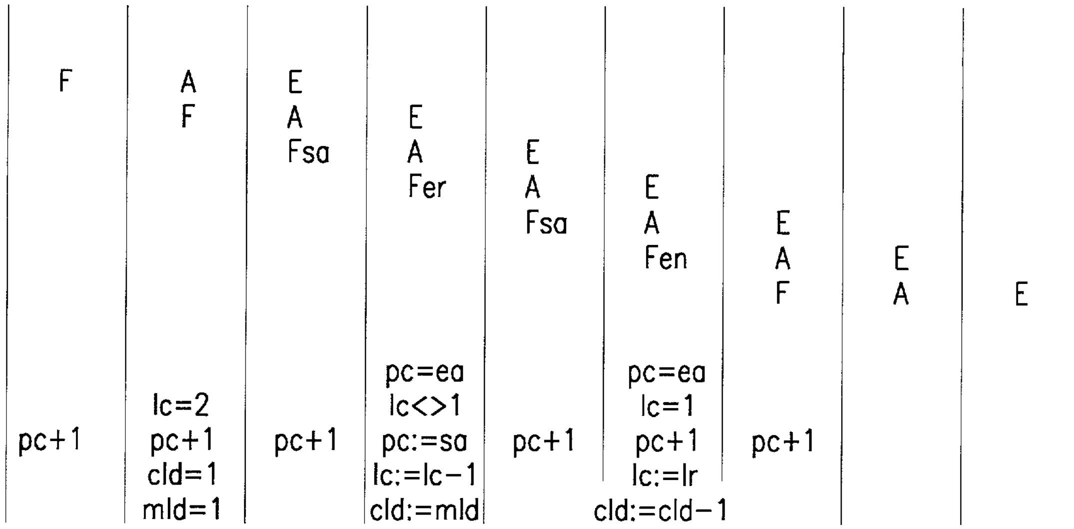


Fcm – CACHE–MISS
Anm – NO MASTER PHASE OF THE ADDRESS UNIT, THUS NO REGISTER MODIFY.
Exb – CROSSBAR ACCESS(ES) OCCUR. STORES COMPLETE TO MEMORY. LOADS COMPLETE INTO TEMPORARY LATCHES, MASTER PHASE OF DATA UNIT OPERATIONS KILLED.
Enm – NO MASTER PHASE OF DATA UNIT.
Fwa – WAIT FOR CACHE–MISS ACKNOWLEDGE FROM TP.
Fpc – TRANSFER PC AND SEGMENT NUMBER TO TP
Fwp – WAIT FOR SUBSEGMENT PRESENT FLAG TO BECOME SET.
EtL – TEMPORARY LATCH DATA (LOADS) COMPLETE INTO DESIGNATION REGISTER(S). DATA UNIT PERFORMS ITS ALU/MPY OPERATIONS.

FIG. 36



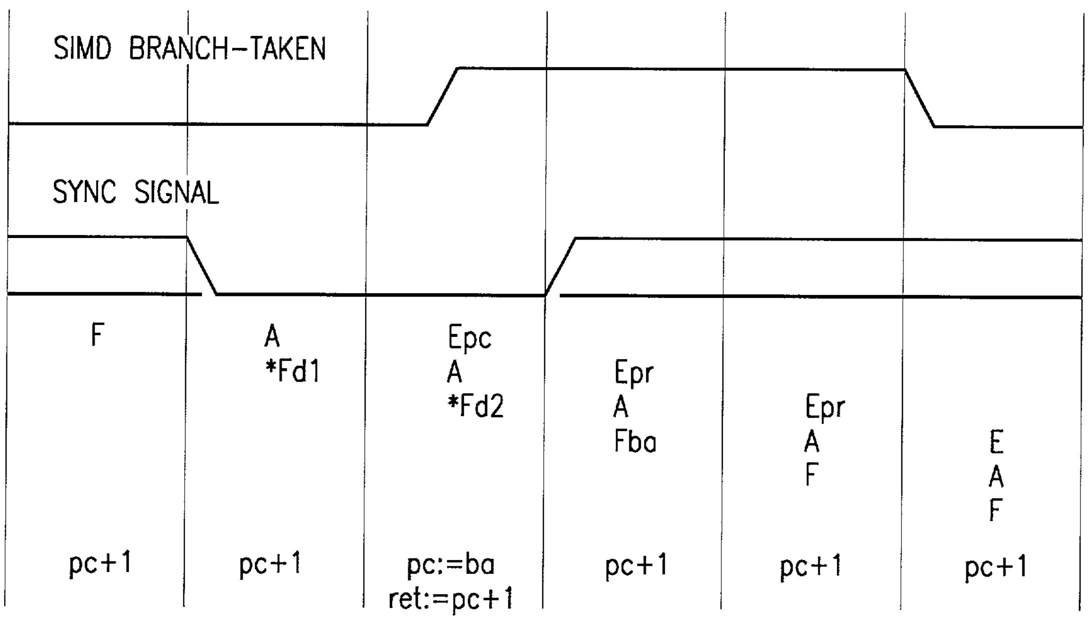
EgL – CONTENTION DETECTED ON BOTH GLOBAL AND LOCAL BUSES. NO MASTER PHASE IN DATA UNIT.
Fnm – NO MASTER PHASE ON FETCH. PIPE NOT LOADED.
Eg – CONTENTION DETECTED ON GLOBAL BUS. LOCAL BUS TRANSFER OCCURS. STORE TO MEMORY, OR LOAD TO TEMP REGISTER. NO MASTER PHASE IN DATA UNIT.
EtL – TEMPORARY LATCH DATA (LOADS) COMPLETE INTO DESTINATION REGISTER(S). DATA UNIT PERFORMS ITS ALU/MPY OPERATIONS.
Anm – NO MASTER PHASE IN ADDRESS UNIT. ADDRESS REGISTER NOT MODIFIED.



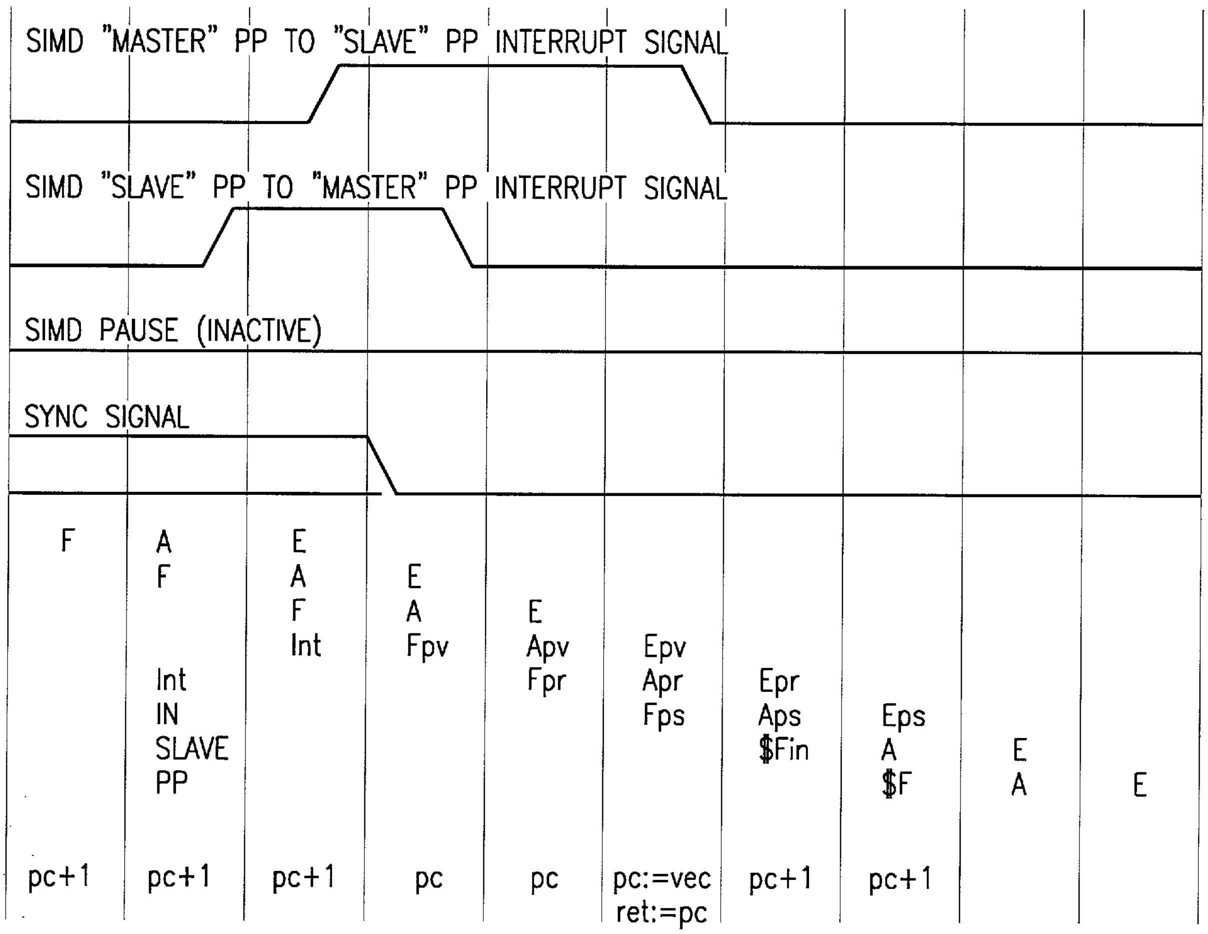
Fsa – START ADDRESS OF LOOP. PC INCREMENTS NORMALLY.
Fer – END ADDRESS, REPEAT LOOP. LOOP COUNTER NOT ONE. LOAD PC WITH START ADD.
Fen – END ADDRESS, NO-REPETITION. LOOP COUNTER IS ONE. PC INCREMENTS NORMALLY.

FIG. 37

FIG. 38

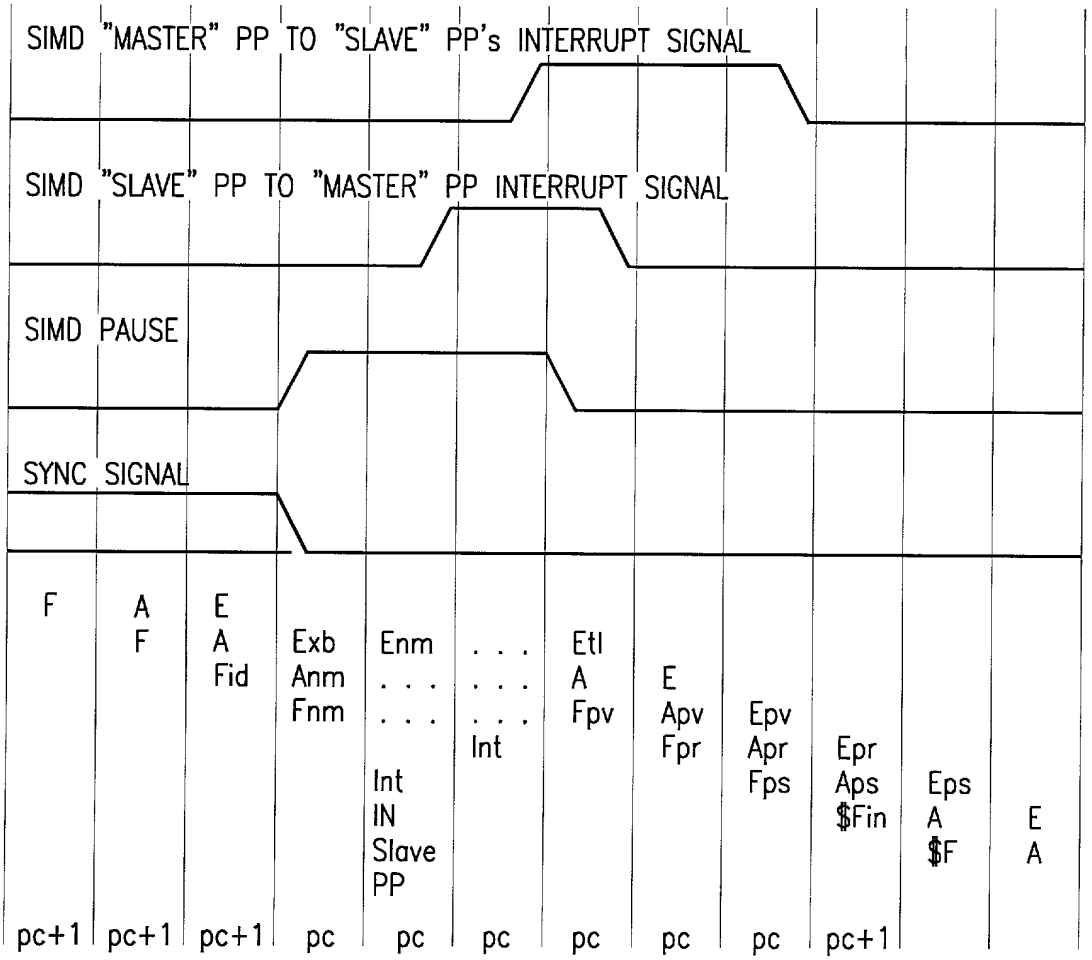


Epc – COPY PC+1 INTO RET. LOAD PC WITH BRANCH ADDRESS.
Epr – PUSH RET IF A CALL. (EITHER Epr CAN PUSH THE RETURN ADDRESS).
Fd1 – DELAY SLOT 1 INSTRUCTION FETCH.
Fd2 – DELAY SLOT 2 INSTRUCTION FETCH.
Fba – FETCH INSTRUCTION FROM BRANCH ADDRESS.
* – INTERRUPTS LOCKED OUT.



Int – INTERRUPT OCCURS.
Fpv – PSEUDO INSTRUCTION. (PC TO RET. VECTOR FETCH INTO PC).
Apv – CALCULATE INTERRUPT VECTOR ADDRESS.
Epv – COPY PC TO RET. FETCH INTERRUPT VECTOR INTO PC.
Fpr – PSEUDO INSTRUCTION. (PUSH RET).
Apr – CALCULATE STACK PUSH ADDRESS.
Epr – PUSH RET ONTO STACK.
Fps – PSEUDO INSTRUCTION. (PUSH SR).
Aps – CALCULATE STACK PUSH ADDRESS.
Eps – PUSH SR ONTO STACK. CLEAR S, I AND CLD BITS IN SR.
Fin – FIRST INSTRUCTION OF INTERRUPT ROUTINE.
$ – SYNC, INTERRUPTS AND LOOPING DISABLED UNTIL AFTER SR HAS BEEN PUSHED. NEITHER OF FIRST TWO INSTRUCTIONS OF INTERRUPT ROUTINE MAY BE A LCK.

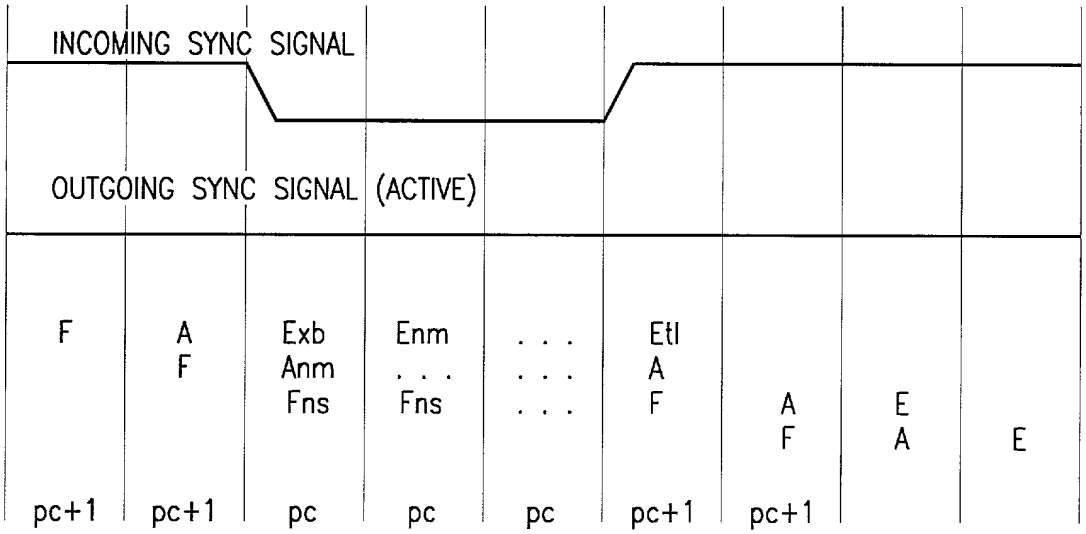
FIG. 39



Fid – IDLE INSTRUCTION FETCHED.
Fnm – NO MASTER PHASE ON INSTRUCTION FETCH. PIPELINE NOT LOADED.
Anm – NO MASTER PHASE ON INSTRUCTION FETCH. ADDRESS REGISTERS NOT MODIFIED.
Exb – CROSSBAR ACCESS(ES) OCCUR. STORES COMPLETE TO MEMORY. LOADS COMPLETE INTO TEMPORARY LATCHES. MASTER PHASE OF DATA UNIT OPERATIONS KILLED.
Enm – NO MASTER PHASE IN DATA UNIT.
Int – INTERRUPT OCCURS.
EtL – TEMPORARY LATCH DATA (LOADS) COMPLETE INTO DESTINATION REGISTER(S). DATA UNIT PERFORMS ITS ALU/MPY OPERATIONS.
Fpv – PSEUDO INSTRUCTION. (PC TO RET. VECTOR FETCH INTO PC).
Apv – CALCULATE INTERRUPT VECTOR ADDRESS.
Epv – COPY PC TO RET. FETCH INTERRUPT VECTOR INTO PC.
Fpr – PSEUDO INSTRUCTION. (PUSH RET).
Apr – CALCULATE STACK PUSH ADDRESS.
Epr – PUSH RET ONTO STACK.
Fps – PSEUDO INSTRUCTION. (PUSH SR).
Aps – CALCULATE STACK PUSH ADDRESS.
Eps – PUSH SR ONTO STACK. CLEAR S, I AND CLD BITS IN SR.
Fin – FIRST INSTRUCTION OF INTERRUPT ROUTINE.
$ – SYNC, INTERRUPTS AND LOOPING DISABLED UNTIL AFTER SR HAS BEEN PUSHED. NEITHER OF FIRST TWO INSTRUCTIONS OF INTERRUPT ROUTINE MAY BE A LCK.

FIG. 40

FIG. 41



Fns – NO SYNC CONDITION. PIPE NOT LOADED. PC UNALTERED.
Anm – NO MASTER PHASE IN ADDRESS UNIT. ADDRESS REGISTERS NOT MODIFIED.
Exb – CROSSBAR ACCESS(ES) OCCUR. STORES COMPLETE TO MEMORY. LOADS COMPLETE INTO TEMPORARY LATCHES. MASTER PHASE OF DATA UNIT OPERATIONS KILLED.
Enm – NO MASTER PHASE IN DATA UNIT.
EtL – TEMPORARY LATCH DATA (LOADS) COMPLETE INTO DESIGNATION REGISTER(S). DATA UNIT PERFORMS ITS ALU/MPY OPERATIONS.

FIG. 42

LOADS: (ASSUMING NO SIGN-EXTENSION)

		BYTE NO. 3 2 1 0	
SOURCE DATA:			
0000h	=	D C B A	(MEMORY)
0004h	=	H G F E	
DESTINATION	=	? ? ? ?	(REGISTER)

OP.	ADD.	16-BIT LOADS...	REG VALUE	OP.	ADD.	32-BIT LOADS...	REG VALUE
LD	0000h	0 0 B A	0 0 B A	LD	0000h	D C B A	D C B A
LDU	0002h	– – – –	0 0 B A	LDU	0004h	– – – –	D C B A
LD	0001h	– – – B	? ? ? B	LD	0001h	– D C B	? D C B
LDU	0003h	0 0 C –	0 0 C B	LDU	0005h	E – – –	E D C B
LD	0002h	0 0 D C	0 0 D C	LD	0002h	– – D C	? ? D C
LDU	0004h	– – – –	0 0 D C	LDU	0006h	F E – –	F E D C
LD	0003h	– – – D	? ? ? D	LD	0003h	– – – D	? ? ? D
LDU	0005h	0 0 E –	0 0 E D	LDU	0007h	G F E –	G F E D

STORES:

SOURCE DATA: = D C B A (REGISTER)

DESTINATION DATA: = BYTE NO. 3 2 1 0 — — — —

0000h = ? ? ? ? (MEMORY)
0004h = ? ? ? ?

OP.	ADD.	16-BIT STORES...	0000h 0004h	OP.	ADD.	32-BIT STORES...	REG VALUE
ST	0000h	0 0 B A	? ? B A ? ? ? ?	ST	0000h	D C B A	D C B A ? ? ? ?
STU	0002h	— — — —	? ? B A ? ? ? ?	STU	0004h	— — — —	D C B A ? ? ? ?
ST	0001h	— — A —	? ? A ? ? ? ? ?	ST	0001h	C B A —	C B A ? ? ? ? ?
STU	0003h	— B — —	? B A ? ? ? ? ?	STU	0005h	— — — D	C B A ? ? ? ? D
ST	0002h	— A — —	? A ? ? ? ? ? ?	ST	0002h	B A — —	B A ? ? ? ? ? ?
STU	0004h	B — — —	B A ? ? ? ? ? ?	STU	0006h	— — D C	B A ? ? ? ? D C
ST	0003h	A — — —	A ? ? ? ? ? ? ?	ST	0003h	A — — —	A ? ? ? ? ? ? ?
STU	0005h	— — — B	A ? ? ? ? ? ? B	STU	0007h	— D C B	A ? ? ? ? D C B

FIG. 43

ADD WITH SATURATE

```
ADDM    D0, D1, D2
MRGM    D2, D3, D2

 D0 = 89 23 CD 67
+D1 = 01 AB 45 EF
-----------------
 D2: = 8A CE 12 56
MFLAGS: = ?? ?? ?? ?3

 D2 = 8A CE 12 56
 D3 = FF FF FF FF
-----------------
 D2: = 8A CE FF FF
```

MAXIMUM

```
SUBM    D0, D1, D2
MRGM    D0, D1, D2

 D0 = 89 23 CD 67
-D1 = 01 AB 45 EF
-----------------
 D2: = 88 67 88 67
MFLAGS: = ?? ?? ?? ?5

 D0 = 89 23 CD 67
 D1 = 01 AB 45 EF
-----------------
 D2: = 89 AB CD EF
```

TRANSPARENCY

```
CMPM    D0, D1
MRGM    D0, D2, D3

 D0 = 89 23 CD 67
(-)D1 = 23 23 23 23
-------------------
   (= 66 00 8A 44)
MFLAGS: = ?? ?? ?? ?4

 D0 = 89 23 CD 67
 D2 = 87 65 43 21
-----------------
 D3: = 89 65 CD 67
```

COLOUR EXPANSION

```
  LD    *A0, MFLAGS
MRGM    D0, D1, D2

MFLAGS = XX XX XX X6

 D0 = 11 11 11 11
 D1 = 88 88 88 88
-----------------
 D2: = 11 88 88 11
```

COLOUR COMPRESSION

```
CMPM    D0, D1, D2

 D0 = 89 23 CD 67
(-)D1 = 89 89 89 89
-------------------
   (= 00 89 44 CD)
MFLAGS = ?? ?? ?? ?8
```

GUIDED COPY

```
  LD    *A0, MFLAGS
MRGM    D0, D1, D1

MFLAGS = XX XX XX XC

 D0 = 89 23 CD 67
 D1 = 87 65 43 21
-----------------
 D1: = 87 65 CD 67
```

FIG. 44

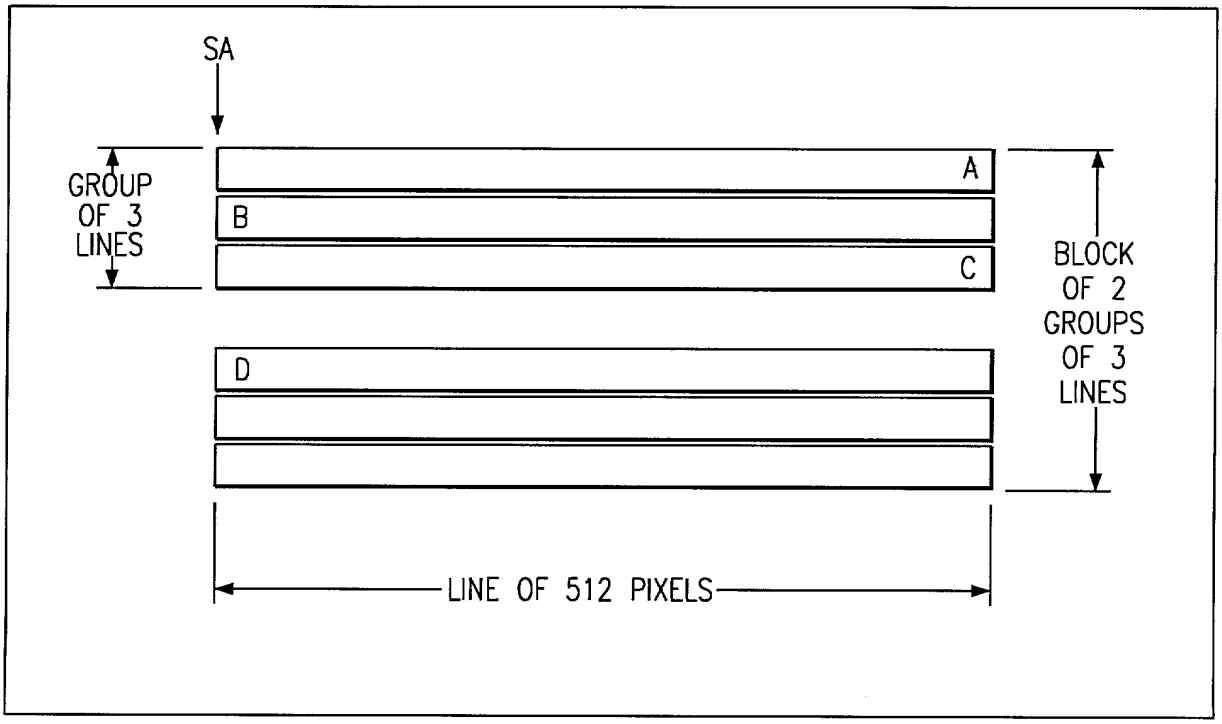


FIG. 45

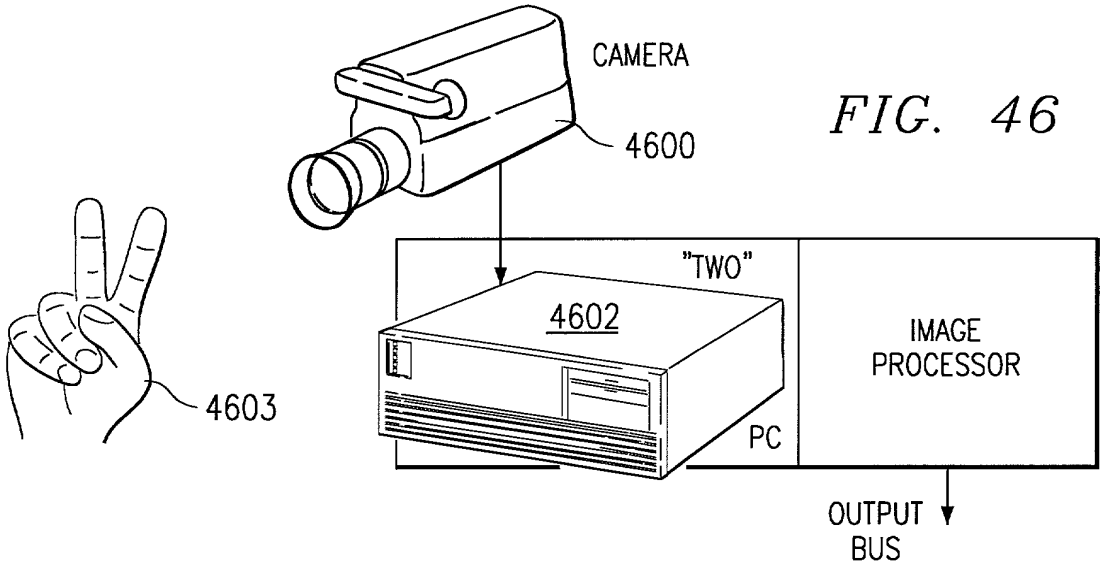


FIG. 46

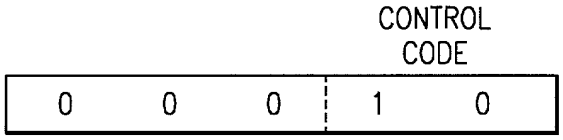


FIG. 47

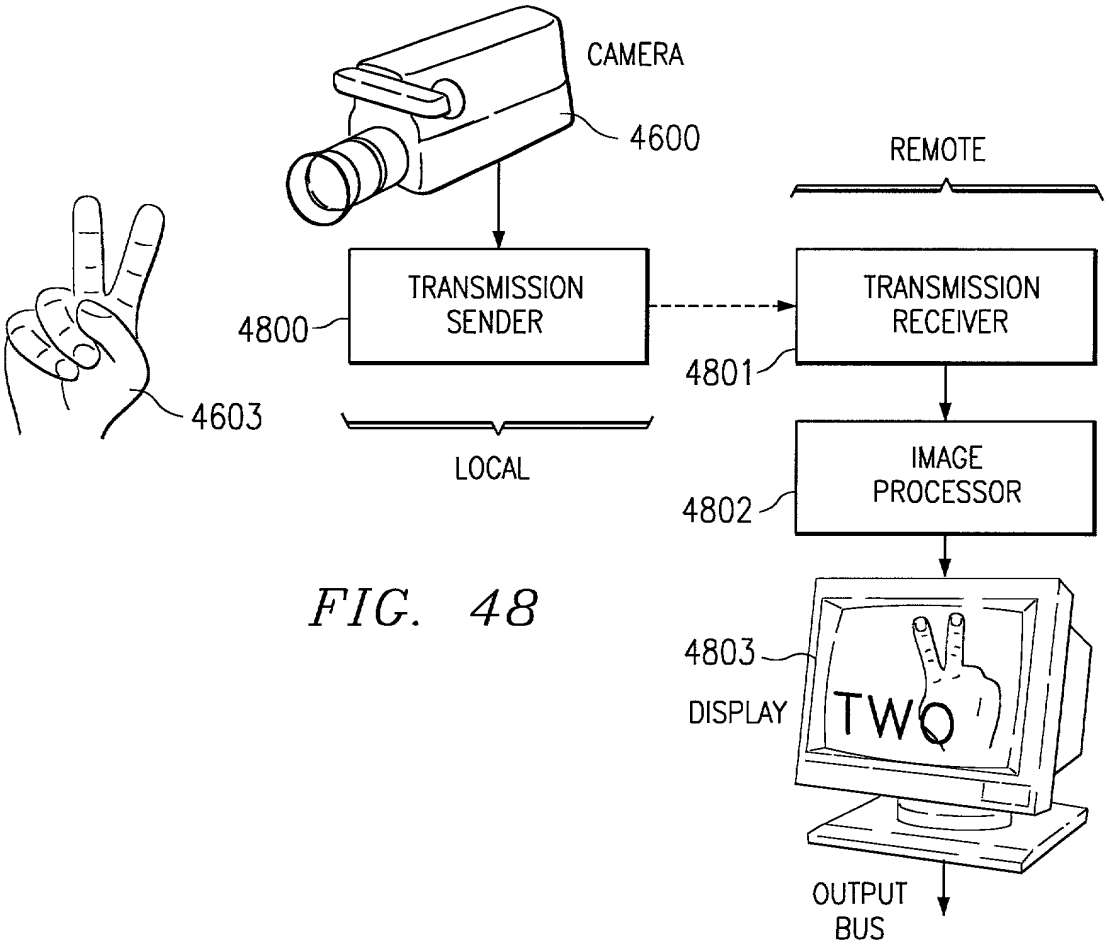


FIG. 48

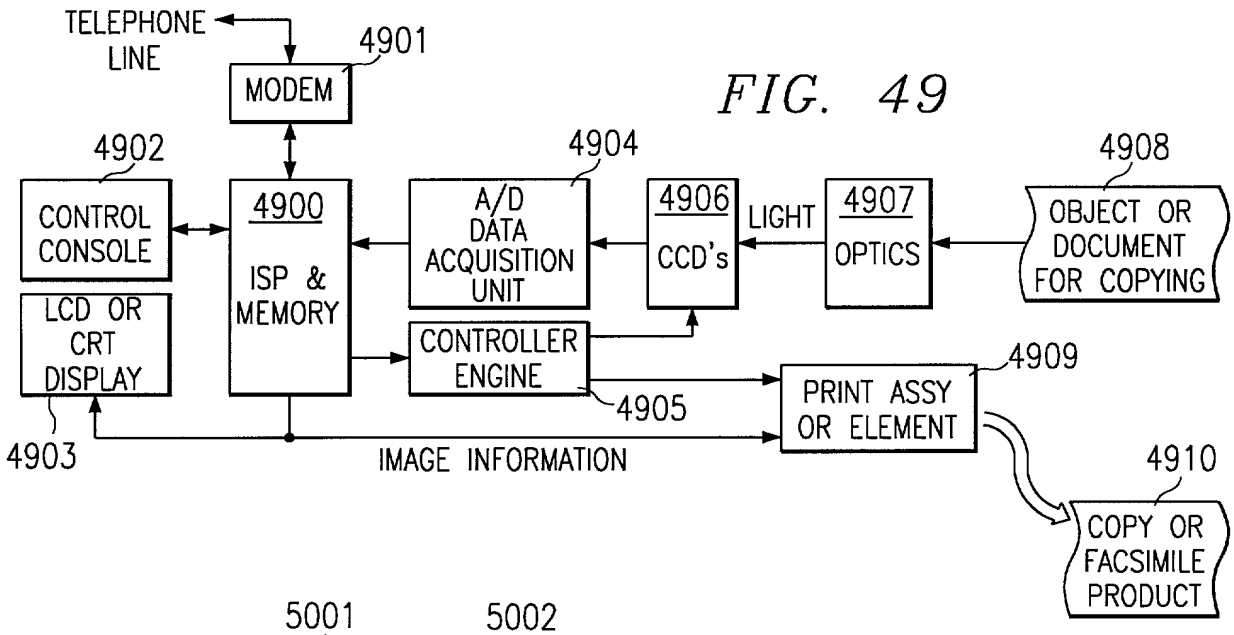


FIG. 49

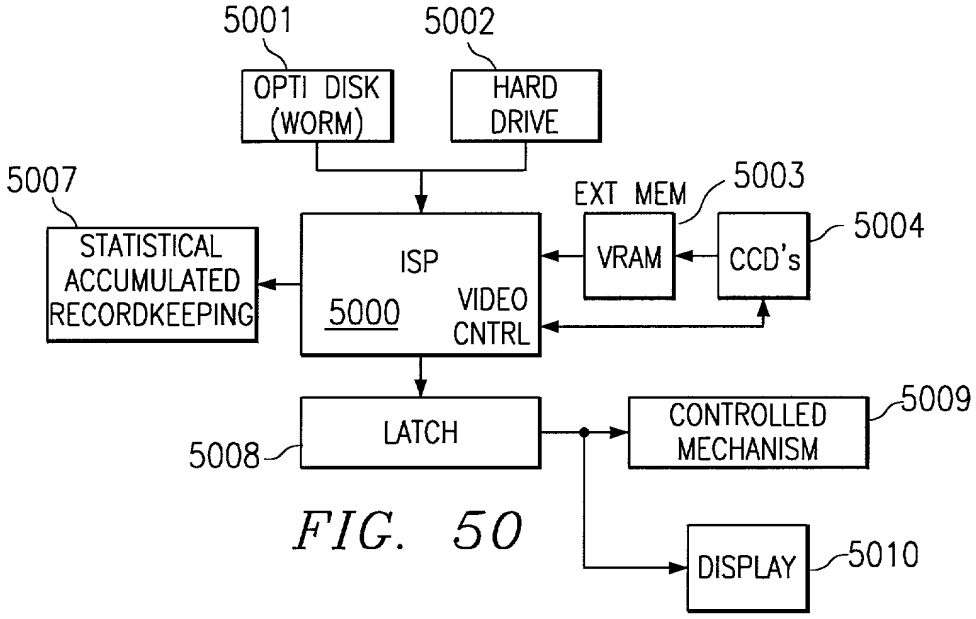


FIG. 50

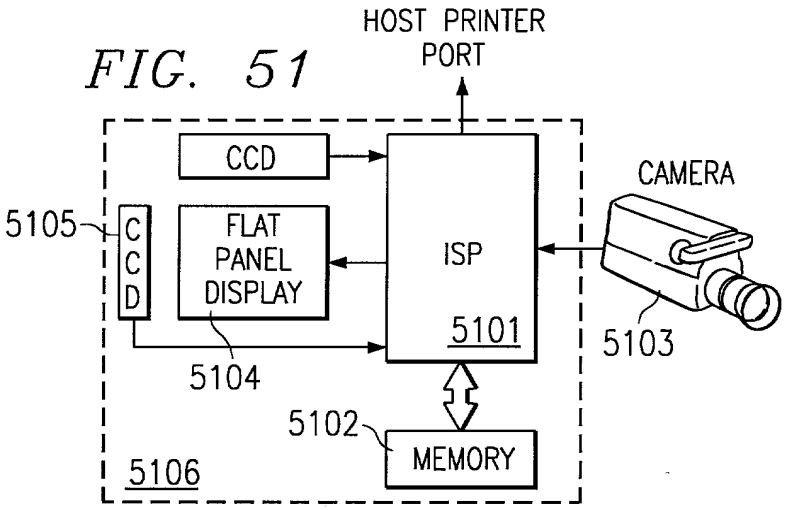


FIG. 51

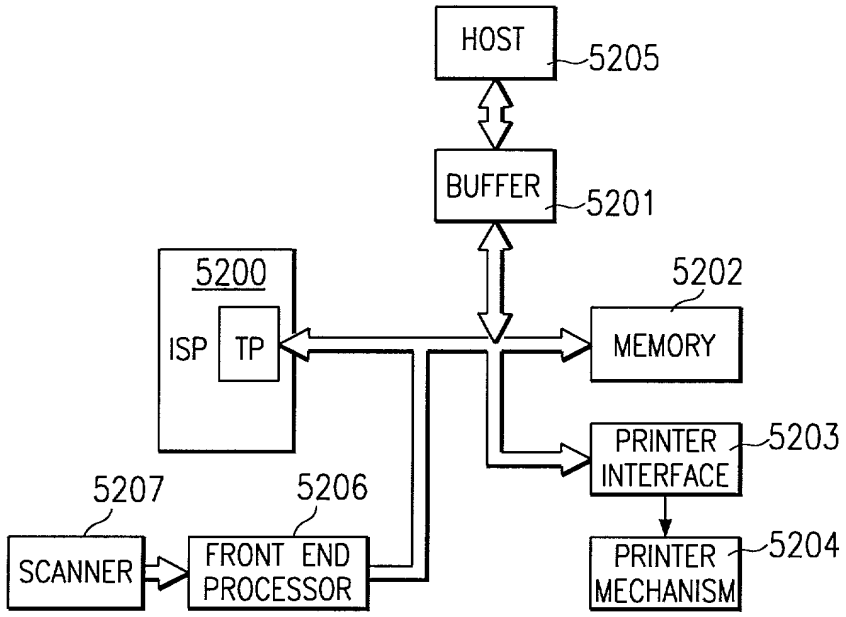

HOST
5205
BUFFER
5201
5200
ISP
TP
5202
MEMORY
PRINTER INTERFACE
5203
5207
5206
SCANNER
FRONT END PROCESSOR
PRINTER MECHANISM
5204

FIG. 52

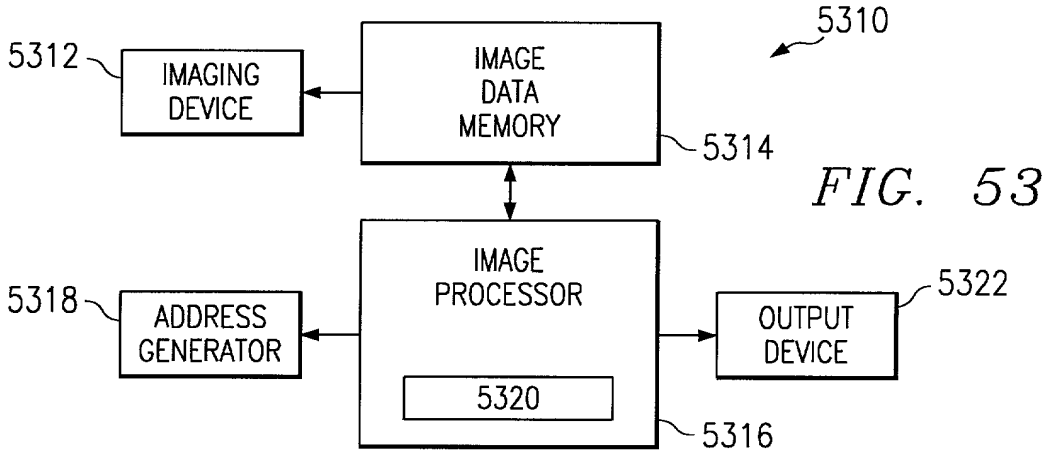

5310
5312
IMAGING DEVICE
IMAGE DATA MEMORY
5314
IMAGE PROCESSOR
5318
ADDRESS GENERATOR
5320
OUTPUT DEVICE
5322
5316

FIG. 53

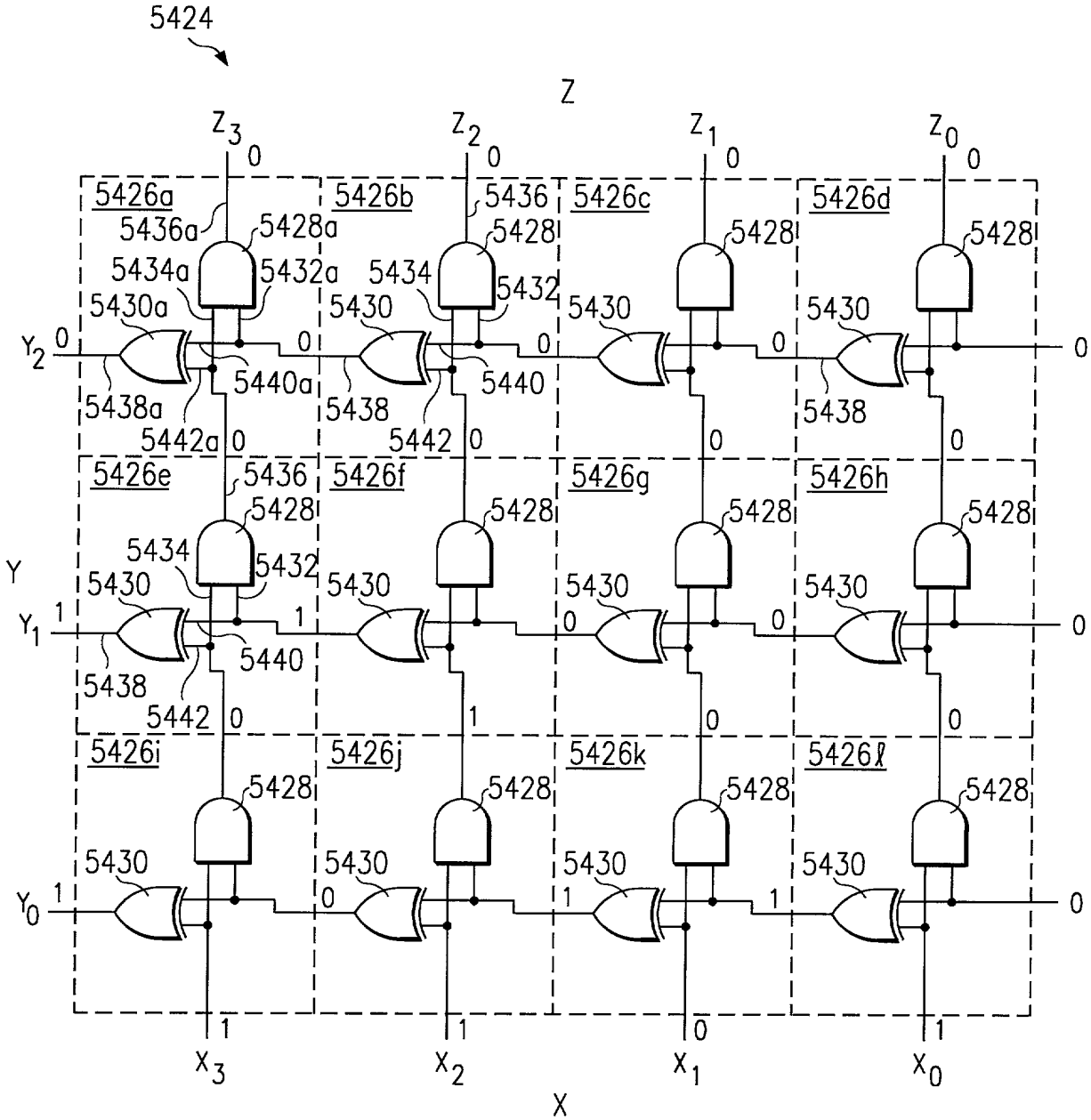

5424
Z
Z3
Z2
Z1
Z0
5426a
5426b
5426c
5426d
5436a
5428a
5436
5428
5434a
5432a
5434
5432
5430a
5430
5438a
5440a
5438
5440
5442a
5442
Y2
Y
Y1
Y0
5426e
5426f
5426g
5426h
5426i
5426j
5426k
5426l
X3
X2
X1
X0
X

FIG. 54

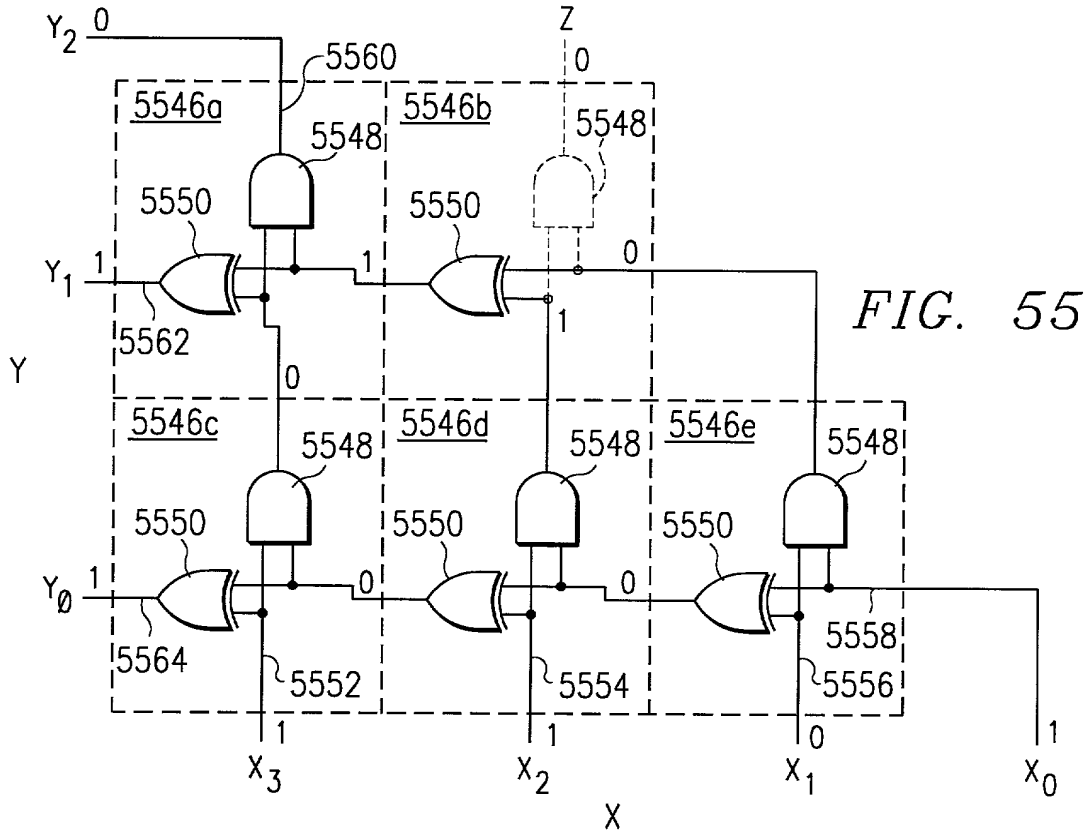


FIG. 55

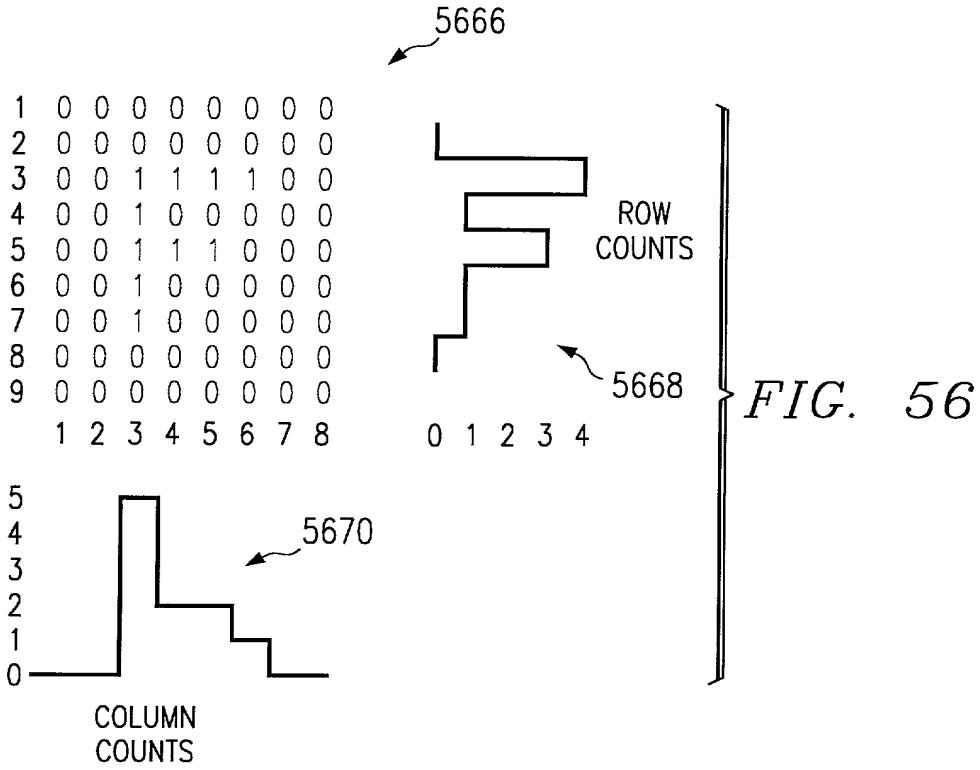


FIG. 56

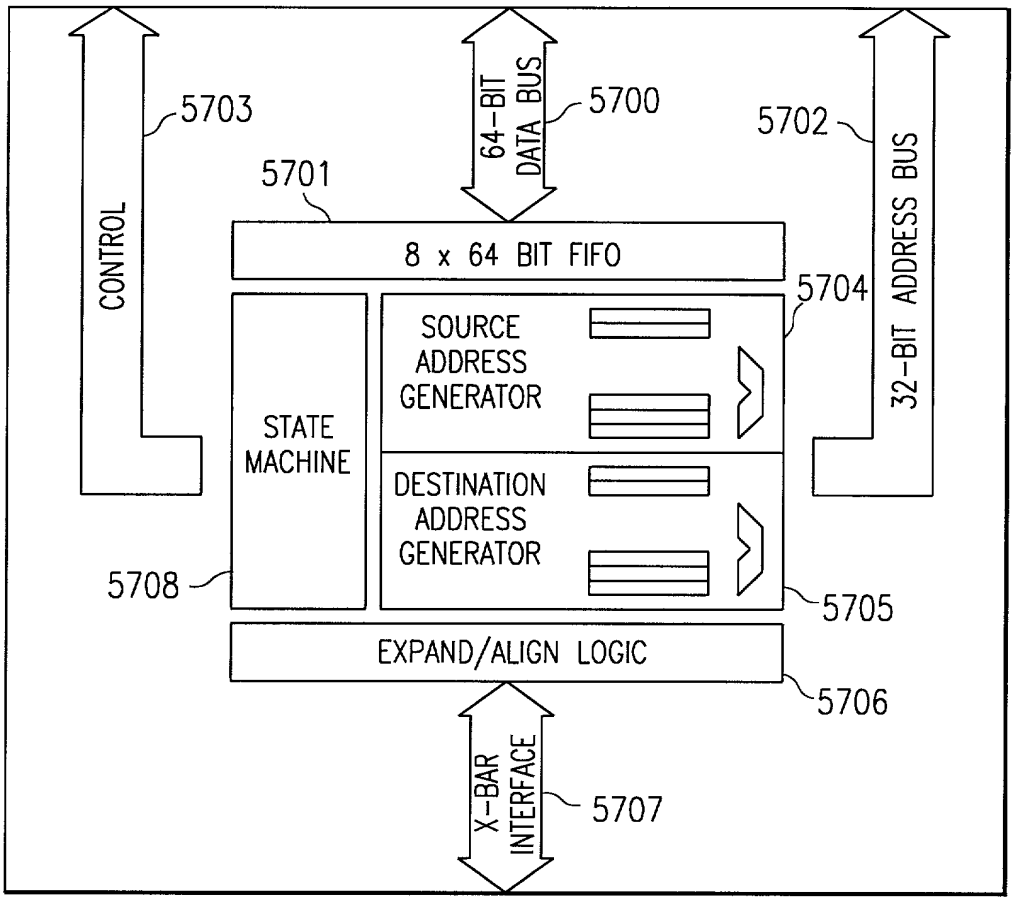

CONTROL
5703
64-BIT DATA BUS
5700
5702
32-BIT ADDRESS BUS
5701
8 x 64 BIT FIFO
5704
STATE MACHINE
SOURCE ADDRESS GENERATOR
DESTINATION ADDRESS GENERATOR
5708
5705
EXPAND/ALIGN LOGIC
5706
X-BAR INTERFACE
5707

FIG. 57

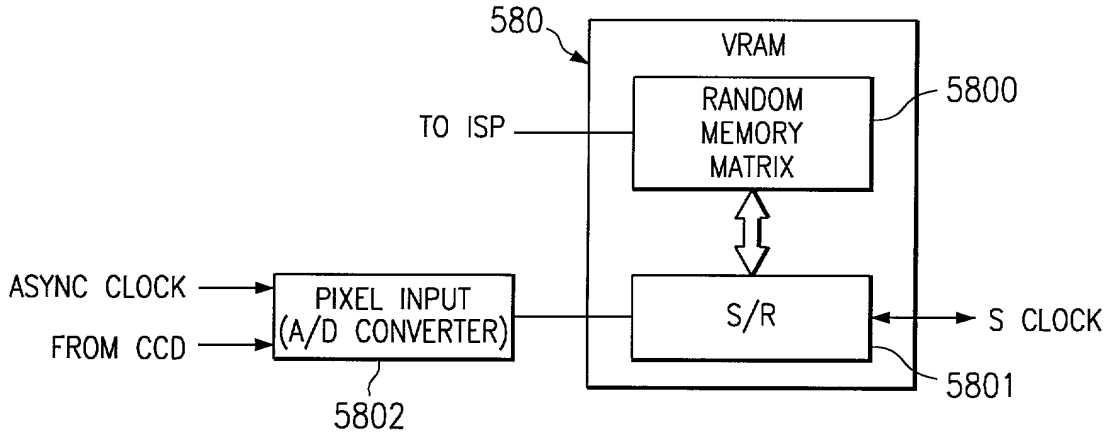

580
VRAM
TO ISP
RANDOM MEMORY MATRIX
5800
ASYNC CLOCK
FROM CCD
PIXEL INPUT (A/D CONVERTER)
S/R
S CLOCK
5801
5802

FIG. 58

FIG. 59
(PRIOR ART)

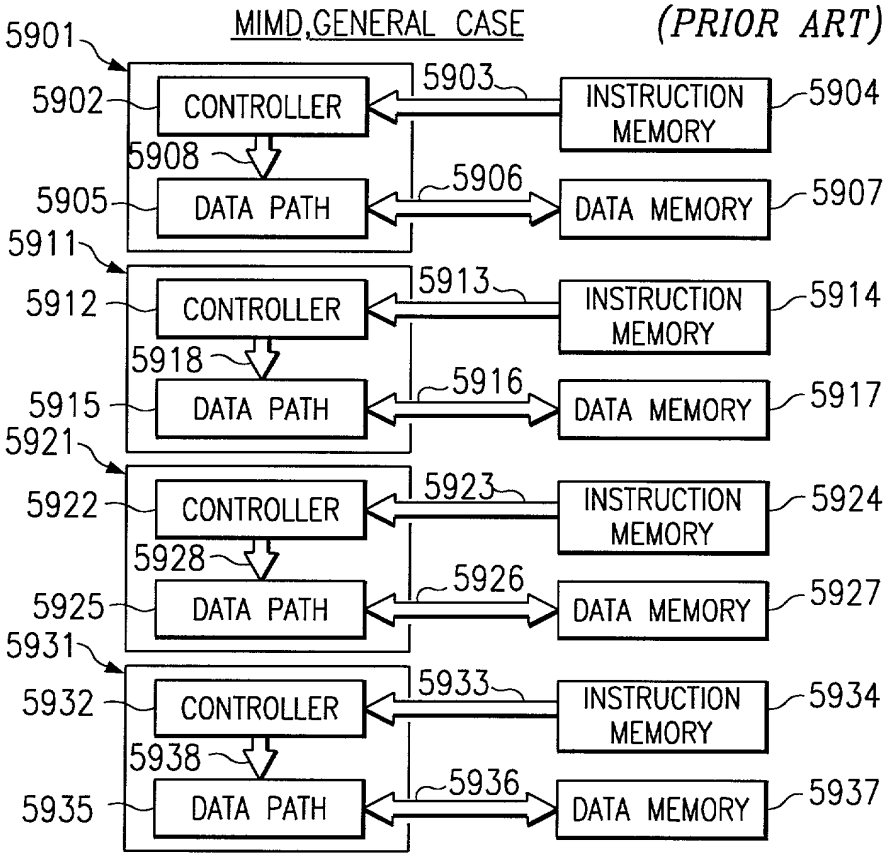
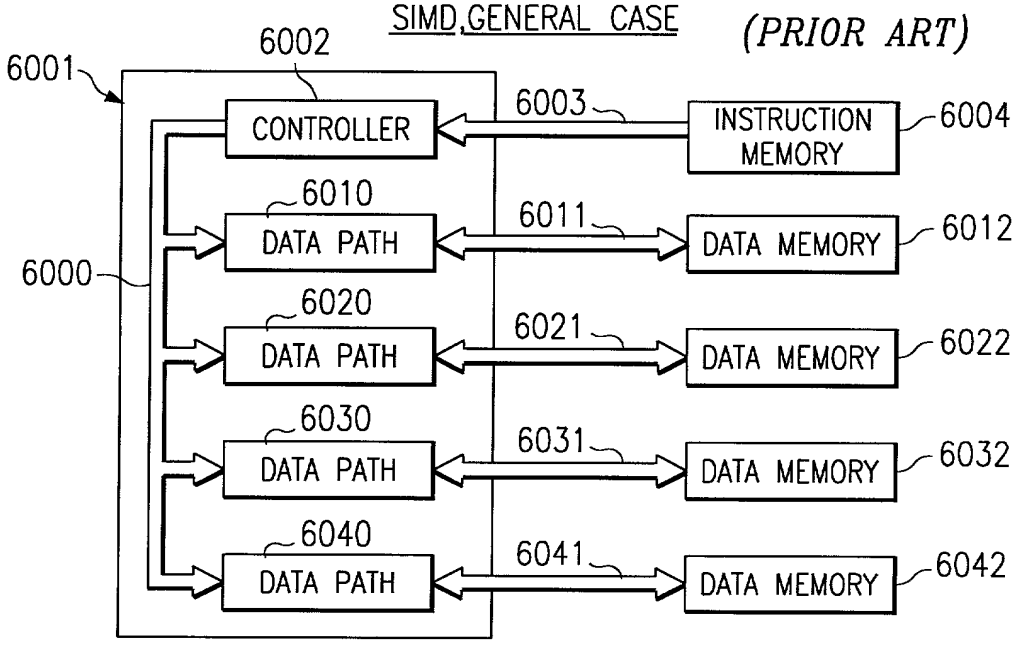


FIG. 60
(PRIOR ART)



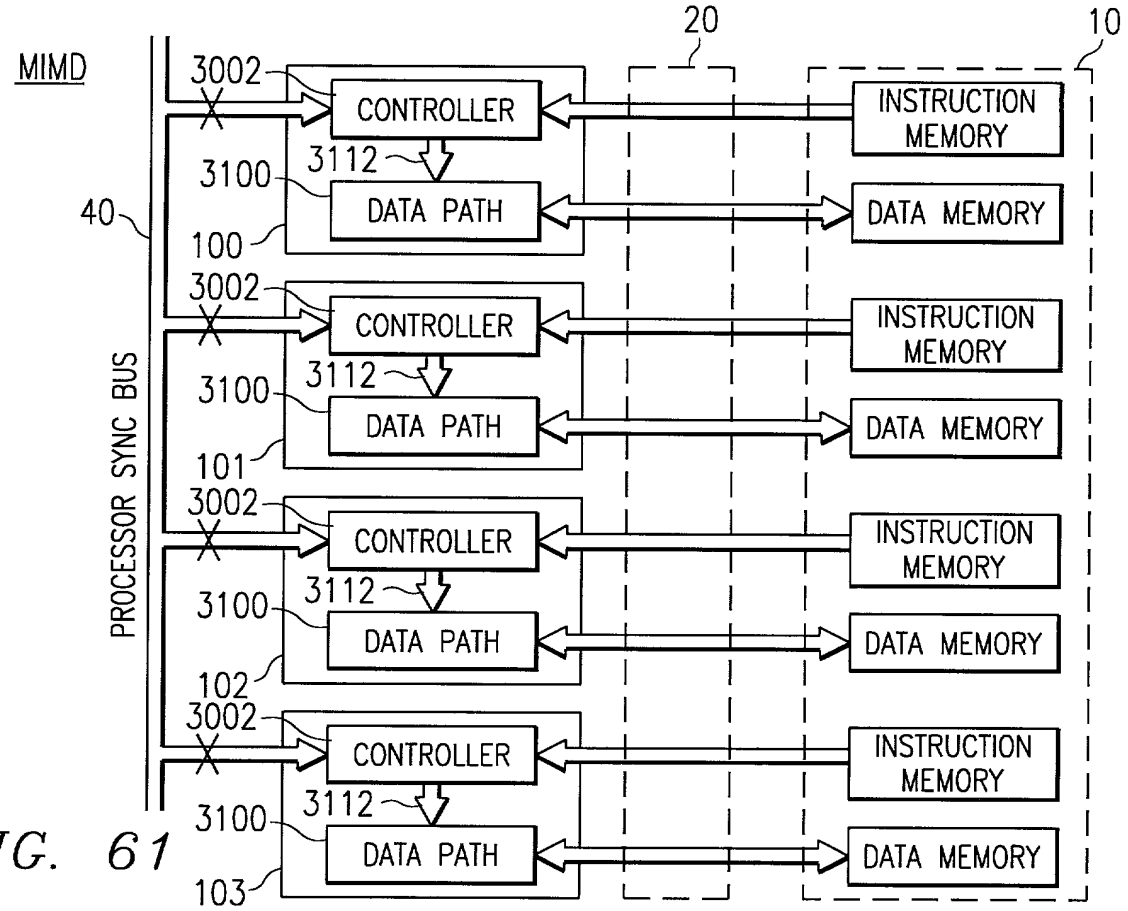

MIMD
20
10
3002
CONTROLLER
INSTRUCTION MEMORY
3112
3100
DATA PATH
DATA MEMORY
40
100
101
102
103
PROCESSOR SYNC BUS

FIG. 61

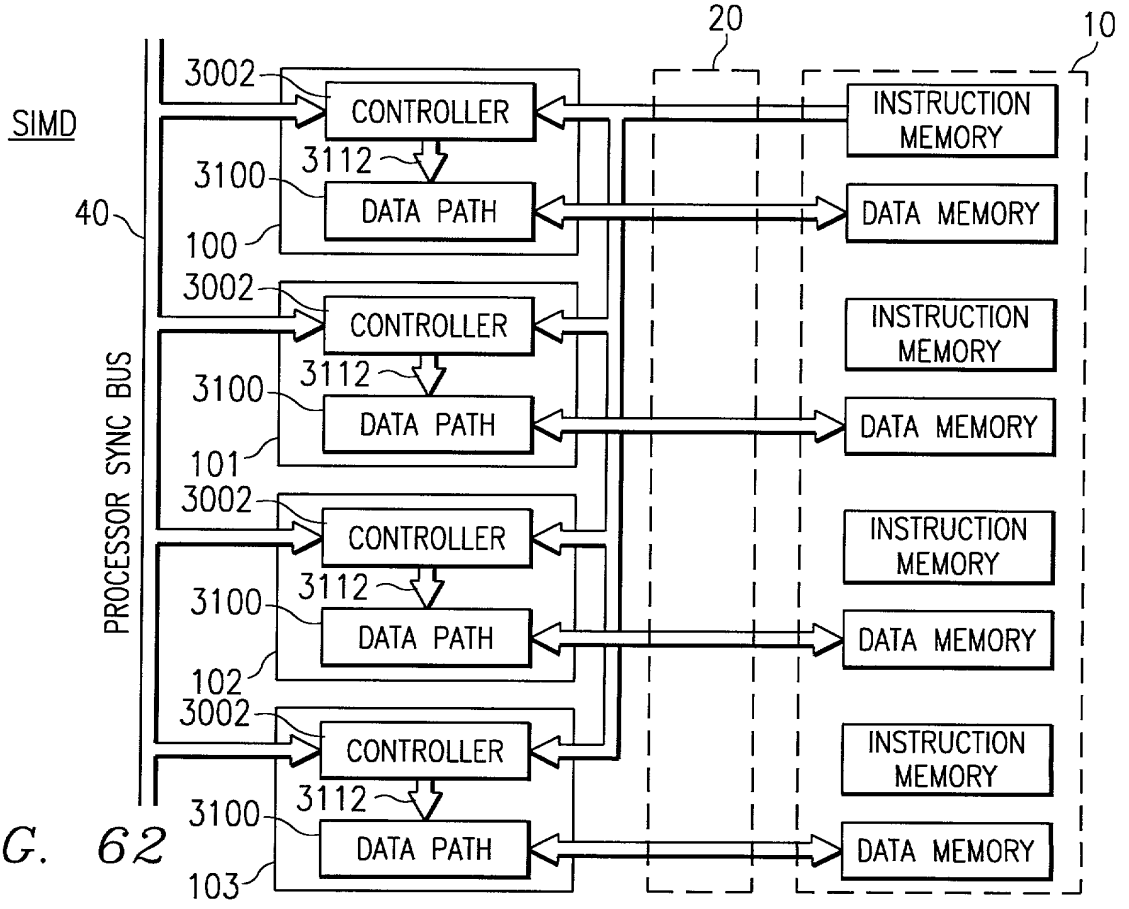

SIMD
20
10
3002
CONTROLLER
INSTRUCTION MEMORY
3112
3100
DATA PATH
DATA MEMORY
40
100
101
102
103
PROCESSOR SYNC BUS

FIG. 62

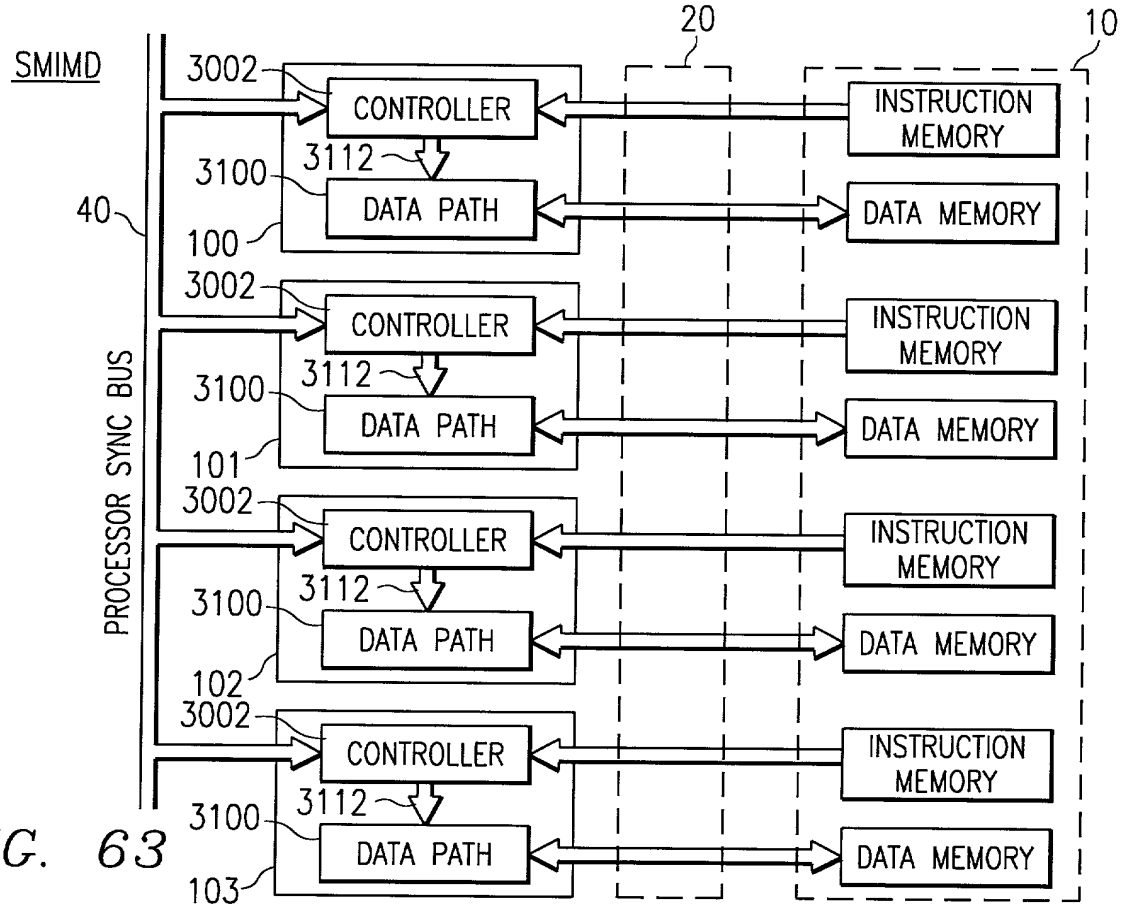

SMIMD
20
10
3002
CONTROLLER
INSTRUCTION MEMORY
3112
3100
DATA PATH
DATA MEMORY
40
100
PROCESSOR SYNC BUS
101
102
103

FIG. 63

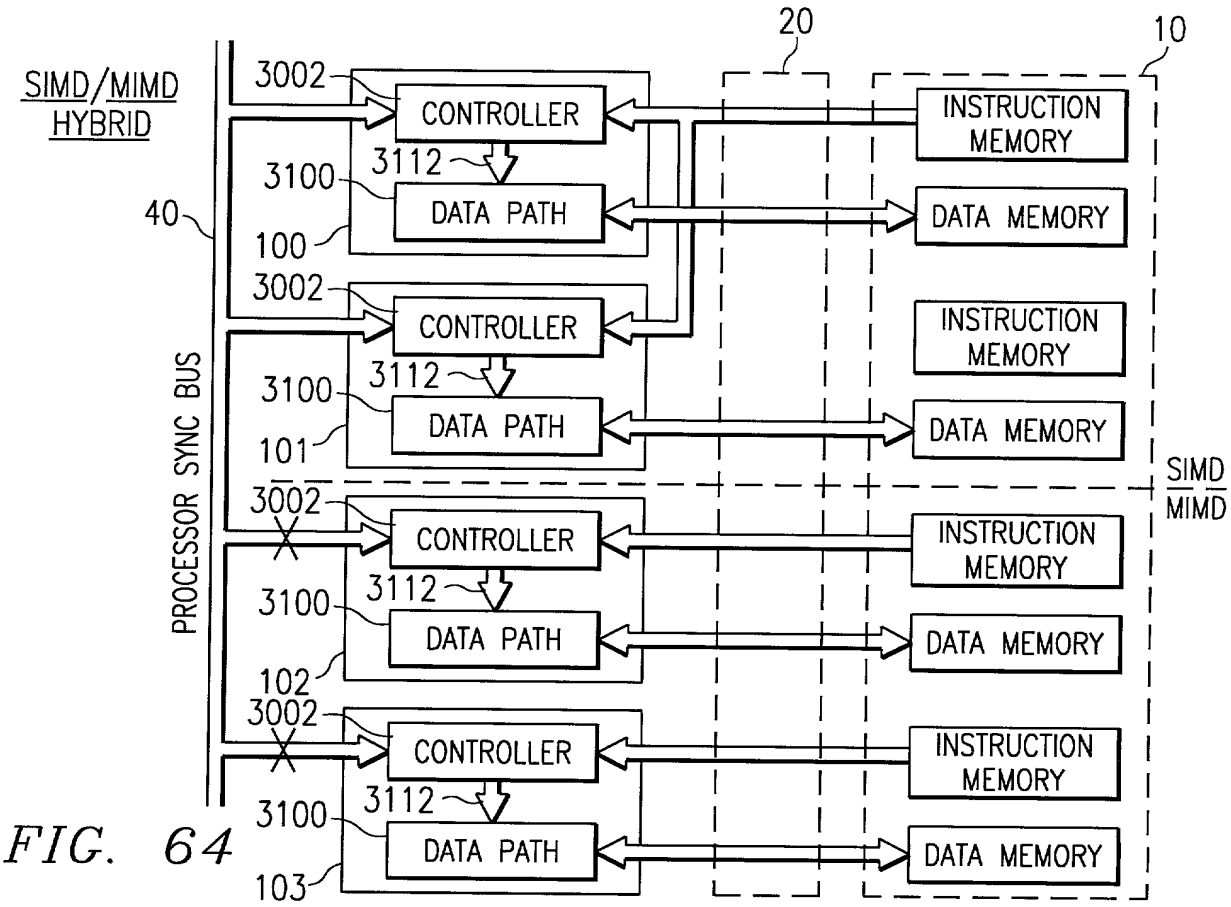

SIMD/MIMD HYBRID
20
10
3002
CONTROLLER
INSTRUCTION MEMORY
3112
3100
DATA PATH
DATA MEMORY
40
100
PROCESSOR SYNC BUS
101
SIMD
MIMD
102
103

FIG. 64